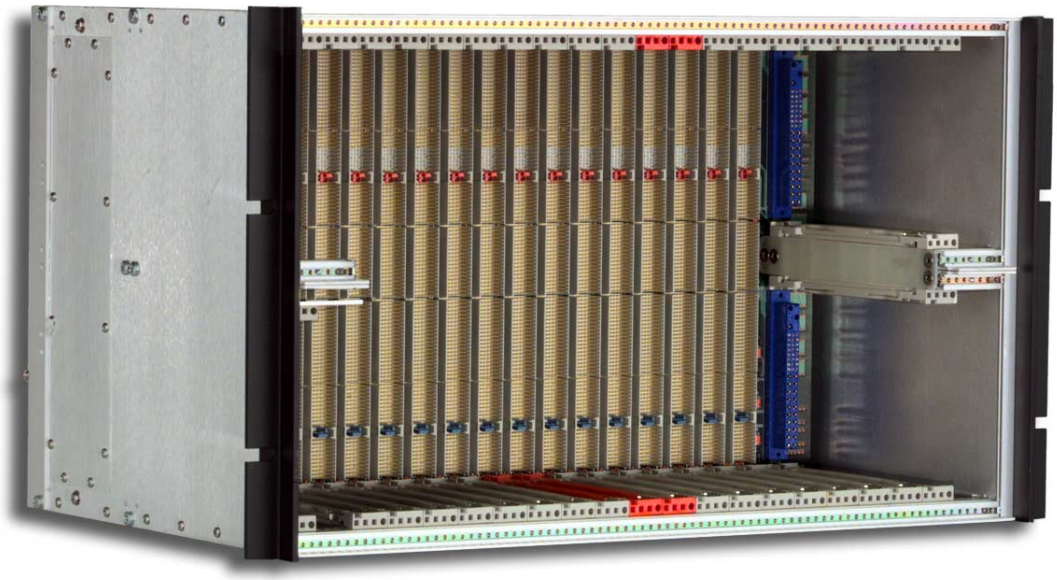
PATTON Electronics Co.

600 Series
6U CPCI Redundant Back-plane/Midplane & Chassis

User Manual



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Contents

About this guide

This manual is a comprehensive hardware reference tool for the Patton Electronics 6U CPCI Redundant Backplane/Midplane and Chassis line of products.

Audience

This guide is intended for the following users:

- System developers installing and integrating the products into their systems
- Operators
- Installers
- Maintenance technicians

Structure

This guide contains the following chapters and appendices:

- Chapter 1, "Introduction"—provides an overview of the product, about Patton Electronics, warranty, and service information.
- Chapter 2, "Chassis specifications"—provides an overview of the chassis features.
- Chapter 3, "Installation checklist"—provides a quick set-up checklist for installing the Model 600.
- Chapter 4, "System Architecture"—provides an overview of CompactPCI specifications, as well as a more in-depth description of the product's features.
- Chapter 5, "CT H.110 Bus Architecture"—defines the CT Bus configured on the J4/P4 connector, when applicable.
- Chapter 6, "Maintenance"—provides a quick set-up checklist, tips for troubleshooting, warranty information, and where to get help.
- Appendix A, "Glossary of Terms"—defines terms and acronyms used in this document.

For best results, read the contents of this guide *before* you install the enclosure.

Precautions

Notes and cautions, which have the following meanings, are used throughout this guide to help you become aware of potential problems. *Warnings* relate to personal injury issues, and *Cautions* refer to potential property damage.

Note Calls attention to additional or noteworthy information or tips.

The shock hazard symbol and WARNING heading indicate a potential electric shock hazard. Strictly follow the warning instructions to avoid injury caused by electric shock.

The alert symbol and WARNING heading indicate a potential safety hazard. Strictly follow the warning instructions to avoid personal injury.

The shock hazard symbol and CAUTION heading indicate a potential electric shock hazard. Strictly follow the instructions to avoid property damage caused by electric shock.

The alert symbol and CAUTION heading indicate a potential hazard. Strictly follow the instructions to avoid property damage.

This symbol and the CAUTION heading indicates a situation where damage to equipment can be caused by electrostatic discharge.

This symbol and the IMPORTANT heading provides information which should be followed for best results when installing, configuring, or operating the Patton product.

Style conventions used in this document

Tables contain information of a descriptive nature. For example, pin assignments or signal description.

Cross-references, figure titles, and table titles are in italicized and hyperlinked. This means that if you have the on-line version of this document, you can click on the cross-reference and it will "jump" you to that reference within the document. This feature only works with references to sections/tables/figures within this document. References to other documents (for example, *PICMG 2.5 R1.0 CompactPCI Computer Telephony Specification*) are not hyperlinked.

The symbols "/" and "#" indicate signals that are active low.

Specific safety-related terms, traceable to certain safety regulatory agency requirements (i.e., IEC950 and harmonized derivative specifications) are used within this manual. Refer to the referenced document for a definition of these terms.

Typographical conventions used in this document

This section describes the typographical conventions and terms used in this guide.

General conventions

The procedures described in this manual use the following text conventions:

Table 1. General conventions

Convention	Meaning
Futura bold type	Indicates the names of menu bar options.
Italicized Futura type	Indicates the names of options on pull-down menus.
Futura type	Indicates the names of fields or windows.
Garamond bold type	Indicates the names of command buttons that execute an action.
< >	Angle brackets indicate function and keyboard keys, such as <SHIFT>, <CTRL>, <C>, and so on.
`Are you ready?`	All system messages and prompts appear in the `Courier` font as the system would display them.
`% dir *.*`	Bold Courier font indicates where the operator must type a response or command

Mouse conventions

The following conventions are used when describing mouse actions:

Table 2. Mouse conventions

Convention	Meaning
Left mouse button	This button refers to the primary or leftmost mouse button (unless you have changed the default configuration).
Right mouse button	This button refers the secondary or rightmost mouse button (unless you have changed the default configuration).
Point	This word means to move the mouse in such a way that the tip of the pointing arrow on the screen ends up resting at the desired location.
Click	Means to quickly press and release the left or right mouse button (as instructed in the procedure). Make sure you do not move the mouse pointer while clicking a mouse button.
Double-click	Means to press and release the same mouse button two times quickly
Drag	This word means to point the arrow and then hold down the left or right mouse button (as instructed in the procedure) as you move the mouse to a new location. When you have moved the mouse pointer to the desired location, you can release the mouse button.

Bibliography

The following publications are used in conjunction with this manual.

- ECTF H.110 (CT Bus) Specification (Revision 1.0)
- CompactPCI Hot Swap Specification—PICMG 2.12 (Revision 1.0)
- CompactPCI Specification—PICMG 2.0 (Revision 2.1)
- Keying of CompactPCI Boards and Backplanes Specification—PICMG 2.10 (Revision 1.0)
- IEC950, Safety of Information Technology Equipment, including Electrical Business Equipment
- IEC 61076-4-101 (1995-05), Specification for 2mm Connector System
- IEEE 1101.10, IEEE Standard for Additional Mechanical Specifications for Microcomputers using IEEE 1101.1 Equipment Practice

Chapter 1 Introduction

Chapter contents

Product features and benefits

Thank you for purchasing the Patton Electronics 600 Series 6U CPCI Redundant Backplane/Midplane and Chassis. The 600 Series chassis is a 21-slot redundant system. The backplane/midplane provides two, electrically separate, 8-slot CPCI bus segments on P1/P2. It also provides a 17-slot common H.110 bus on P4.

The backplane/midplane is configured to accept four Patton Electronics 3U plug-in supplies for N+1 power redundancy. The system can provide 600 W of online power, with one 200 W hot standby unit for fault tolerant operation. The backplane/midplane supports all feed-through with rear A/B shrouds on RP3, RP4, and RP5, and the 14 layer design provides excellent power distribution and signal integrity.

The 600 Series chassis complies with the *PICMG 2.0 R3.0 CompactPCI Specification*, and *PICMG 2.5, ECTF H.110 (CT Bus) Specification* (Rev. 1.0), making it an excellent choice for redundant, fault tolerant applications

What is CompactPCI?

CompactPCI (Peripheral Component Interconnect) is a high-performance industrial computer platform based on the standard PCI electrical specification in rugged 3U or 6U Eurocard-style packaging, with a high-quality 2mm metric pin and socket connector.

CompactPCI is an open specification supported by the PICMG (PCI Industrial Computer Manufacturers Group), which is a consortium of companies involved in utilizing PCI for embedded applications.

Distinct advantages of CompactPCI (“CPCI”) include:

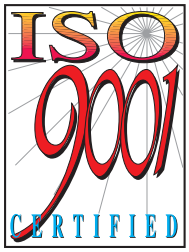
- Cost/time savings—Because it is electrically compatible with PCI, CPCI allows designers to tap into the wealth of available hardware and software. CPCI provides a substantial reduction in engineering and manufacturing costs because off-the-shelf items can be shipped to meet your configuration needs and delivery schedules.
- Rugged and reliable—The Eurocard-style packaging—which includes two-piece shielded connectors for better reliability and vertical card orientation for better cooling—provides a robust system based on a subrack backplane architecture.
- Flexibility—CPCI allows either 32- or 64-bit PCI, plus offers an open architecture. Additional connectors are defined for adding standard or proprietary buses or other needs. Hybrid CPCI systems allow bridging to other buses or custom applications.
- Hot-swap capability—Boards can be hot-swapped without disrupting operation, a critical feature in real-time and high-availability applications.

CompactPCI is rapidly becoming the backbone of today’s high-performance, embedded systems. It is ideally suited for telecommunications, computer telephony, real-time machine control, industrial automation, real-time data acquisition, instrumentation, military systems and other applications requiring high speed computing and modular, robust packaging design.

About Patton Electronics Company

Patton Electronics excels in the design, development and production of Embedded Data Communications and Telecommunications Platforms based on open system bus architecture standards (for example, CPCI and VME). These platforms form a significant part of the infrastructure for today's information technology revolution—including the emergence of new packet-based (IP) global communication networks.

Datacom/Telecom platforms require robust and reliable packaging solutions that address key technology issues, such as line density, thermal management, power distribution, scalability, and regulatory compliance. With an increasing number of applications demanding downtime measured in minutes rather than hours, special consideration has to be given to enclosure system functionality. Patton Electronics' full line of enclosure solutions are designed specifically to meet industry's stringent high availability requirements where redundant operation, quick accessibility and high reliability are essential. Patton has a broad engineering background in the development of these technologies for advanced circuit and packet-switched telecommunications systems running voice, data and video applications for commercial and government customers.



Patton offers a wide range of platforms consisting of standard rack/chassis, high speed backplane, power, thermal management, single board computer (SBC) and alarm/network interface products for commercial, voice/data communications, and government/military system applications. Patton Electronics is ISO-9001 Certified.

Chapter 2 Chassis specifications

Chapter contents

6U CPCI subrack

The 600 Series chassis are modular 6U x 19 inch rackmount subrack-type packaging systems suitable for open bus architectures such as CPCI, or custom bus applications. The rugged, rack-mounted 6U CPCI chassis is ideal for telecom, defense, industrial, and commercial environments, and excels in its ease of access, superior cooling, and power distribution. The base unit is adaptable to a wide array of product configurations.

This chapter details the Model 601 6U chassis with 80mm transition module section. The Model 602 does not have the transition module section, making it only 7.25 inches in maximum depth. A listing of the differences between Models 601 and 602 is provided in section “Materials specifications—Models 601 and 602 chassis” on page 21.

Product features include:

- ✔ Full dimensional compatibility with CompactPCI (PICMG 2.0 R3.0) and IEEE-1101.10.
- ✔ EMI shielding on entire assembly, with continuous chassis ground.
- ✔ Lightweight and durable aluminum construction, suitable for rugged environments.
- ✔ Five standard colors (additional colors are also available). Standard powder coating finish.
- ✔ Front mounting flanges for 19 in. rack mount environments.

Chassis description, front side

The Model 601, CPCI 6U chassis is 10.50 inches high, by 19 inches wide (standard EIA rack mount, with removable rack mount flanges), by 12 inches deep (maximum). There are sixteen 6U x 160mm slots, (see

figure 1) providing two, electrically separate, CPCI bus segments, at the front of the chassis. Front-entry boards, in accordance with PICMG 2.0 R3.0 CompactPCI specifications, are plugged-in at these slots.

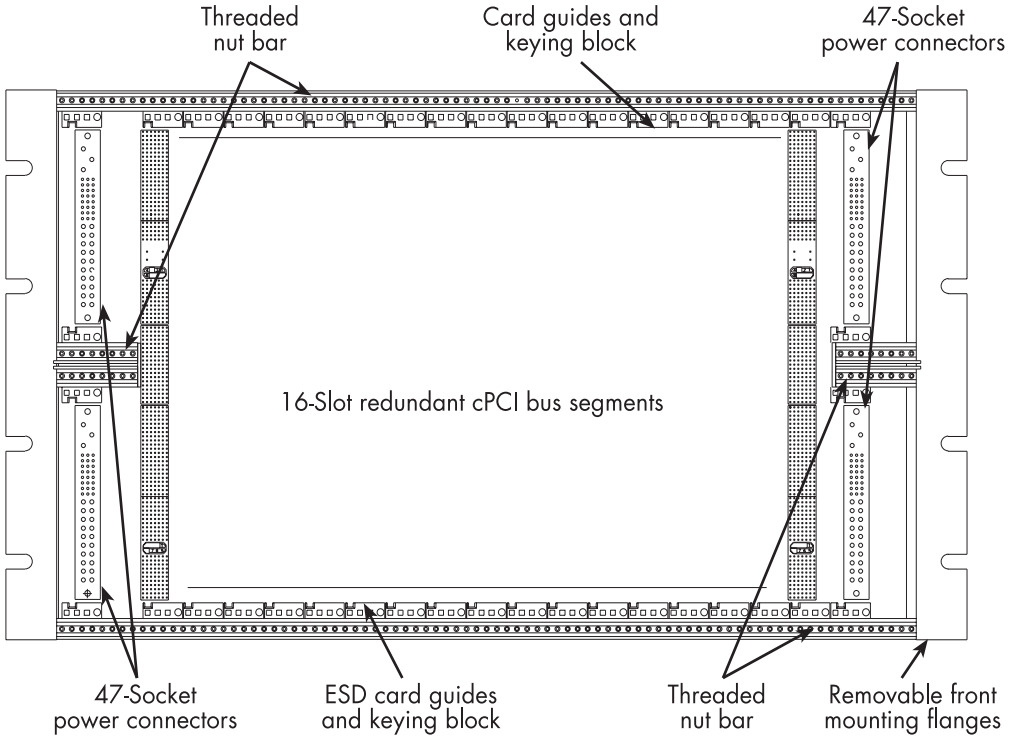


Figure 1. Front view of the Model 601 6U CPCI chassis

The front of the chassis also provides four 3U x 160mm slots to mount up to four Patton power supply modules configured for external DC input, or other CPCI compatible power modules for N+1 power redundancy. The system can provide 600 W of online power, with one 200 W hot standby unit for fault tolerant operation.

Note The chassis guide rails are 1/2HP offset for plug-able power supplies to meet the standards of *PICMG 2.11, R1.0 CompactPCI Power Interface "Draft" Specification*. That is to say, the card guide's slot and injector/ejector PCB mounting surface are shifted 0.1 inch to the right of the card. Card guides are green in color.

All slots provide 4HP module spacing and are on 0.80 in. centers (except for the power connector slots noted above). Card guides are molded plastic with metallic ESD contacts at the bottom of the chassis (see section "Electrostatic discharge (ESD) protection" on page 19) per CompactPCI PICMG 2.0 R3.0 & IEEE 1101.10. Cardguides provide keying and alignment in accordance with IEEE 1101.10, section 8. See "Keying of CPCI backplanes and boards" on page 48 for more information on keying.

Chassis description, rear side

The rear of the Model 601 chassis provides seventeen 6U x 80mm slots for an Alarm card and/or other CPCI transition modules for rear-panel I/O (see figure 2). See “Transition Boards” on page 27 for more information.

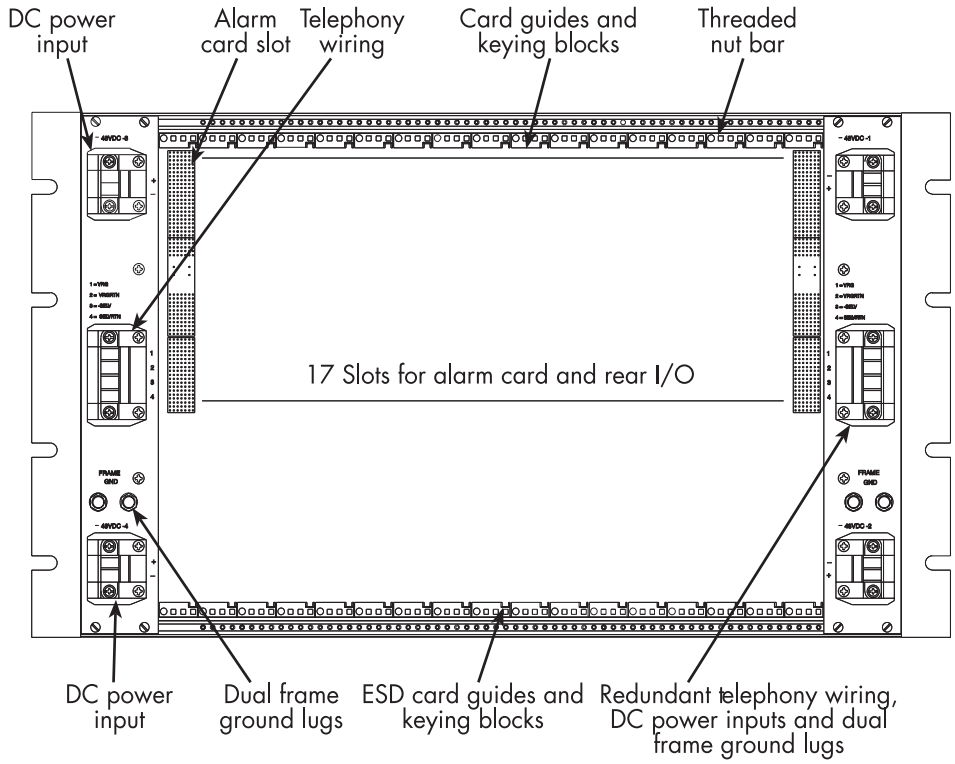


Figure 2. Rear view of the Model 601 6U CPCI chassis

All slots provide 4HP module spacing and are on 0.80 in. centers. Card guides are molded plastic with metallic ESD contacts at the bottom of the chassis (See “Electrostatic discharge (ESD) protection” on page 19) per *CompactPCI PICMG 2.0 R3.0 & IEEE 1101.10*. Cardguides provide keying and alignment in accordance with IEEE 1101.10, section 8. See “Keying of CPCI backplanes and boards” on page 48 for more information on keying.

Note See Table 8 on page 42 for more information on the connectors

Electromagnetic compatibility (EMC)

The 6U Model 601 is an EMC chassis, which reduces the disturbances from EMI as follows:

- All gaskets, contacts, and contact surfaces are electrically conductive
- The mating surfaces of the EMC chassis and the EMC plug-in unit front panels and/or optional EMC filler panels are also conductive by use of gaskets/strips
- All chassis and plug-in contact surfaces are connected to a common chassis ground

Mating EMC gaskets and strips are used on the chassis, front panels of boards, and optional filler panels. An EMC gasket is attached to the left of the chassis (front view), and an EMC strip is attached to the right. Plug-in boards have the corresponding mates on the opposite side (see figure 3).

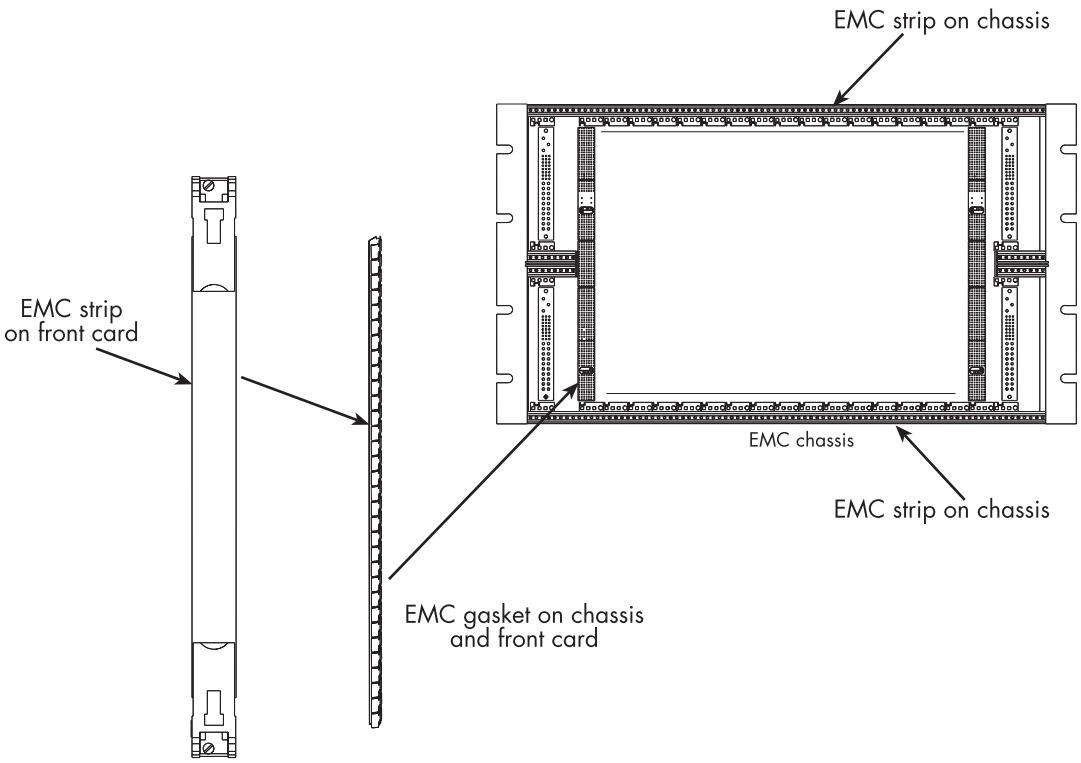


Figure 3. EMC strip and gasket on chassis and cards

The EMC strip on the left side of the board mates with the EMC gasket attached to the chassis when it is plugged into the first slot. Each board mates together with corresponding gaskets/strips.

Note EMC gaskets/strips are in reverse order at the rear of the 6U chassis. That is, the EMC strip is on the left of the chassis and the EMC gasket is on the right. Consequently, rear transition boards are likewise in reverse order to the front-entry boards. The EMC gasket is on the left, and the EMC strip is on the right.

In addition, all aluminum and steel components of the subrack are surface treated and conductive. Top, bottom, sides and rear EMC covers provide mechanical protection and EMC shielding on the subrack. Retaining clips ensure conductive connection.

Electrostatic discharge (ESD) protection

The 6U chassis provides ESD protection in compliance with IEEE 1101.10.

ESD contacts are embedded inside and in the front section of card guides for making early as possible contact with a discharge strip on one or both, the upper and/or lower edge of the plug-in board/module. Only the card

guides located at the bottom rail of the chassis, both front and rear (when there is a transition module present in the chassis), contain the ESD clips. The ESD clip in the card guide is connected to the Chassis GND (ground).

There is an alignment/ESD pin on the injector/ejector handle of boards (see figure 4).

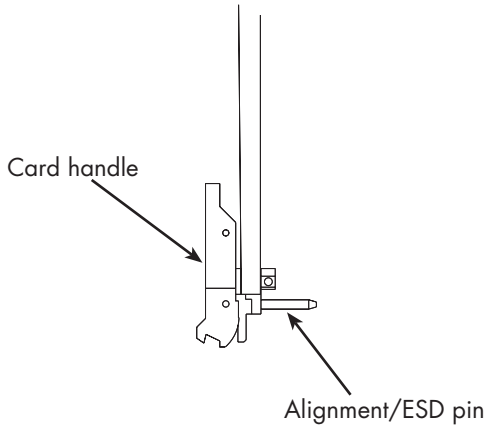


Figure 4. Alignment/ESD pin on card handle

The alignment pin does the following:

- Ensures that the connectors are correctly aligned before they engage
- Provides solid/protected keying
- Provides board ESD contact
- Ensures that the EMC gasket is properly aligned (see “Electromagnetic compatibility (EMC)” on page 18)
- Ensures that when the board is inserted in the card guide, an integrated ESD clip discharges ESD from the board to the right vertical rail chassis ground.

Materials specifications—Models 601 and 602 chassis

A list of the 6U model 601 chassis materials specifications is provided in table 3. A list of the model 602 chassis (which does not have a transition module) materials specifications is provided in table 4.

Table 3. 6U Model 601 chassis materials specifications

Item	Description
Physical	• Height–6U (10.50 in.) • Width–19 in. (standard EIA rack mount) • Depth–12 in. maximum
DC interface	Rear DC interface panel includes dual ground bugs, –48V DC power interface for N+1 redundant power operation, and connectors for VRG, VRGRTN, -SEL VBAT and SEL VBATRTN.
Slot configuration	21 slots (maximum) are on 0.80 in. centers, except power slots are 1.6 in. center • Front—6U x 160 mm slots, Qty: 17 • REAR—6U x 80 mm slots, Qty: 17
module keying and alignment	4HP module spacing, cardguide provides for keying and alignment pin in accordance with IEEE 1101.10, Section 6
Card guides	Molded plastic with snap-in ESD contacts for both plug-in module and injector/ejector handle alignment pin
Plug-in unit injector/ejector handles	Subrack dimensional format accepts modules with injector/ejector handles as specified in IEEE 1101.10, Section 8
6U chassis part no.	60-00001
6U model no.	6001

The Model 602 chassis materials specifications are identical to Model 601 shown above, with the following differences noted in table 4.

Table 4. 6U Model 602 chassis materials specifications

Item	Description
Physical	• Height–6U (10.50 in.) • Width–19 in. (standard EIA rack mount) • Depth–7.25 in. maximum
Slot configuration	21 slots (maximum) are on 0.80 in. centers, except power slots are 1.6 in. center. 17 slots are available when the Model 600 is configures with the 3U power supplies
6U chassis part no.	60-00002
6U model no.	602

Patton Electronics' product interfaces

One of the key features of a CompactPCI system is its interoperability with off-the-shelf boards that have been designed in compliance with the *PICMG CompactPCI 2.0 R2.1 Specification*. The Patton 6U chassis has this built-in interoperability. We believe, however, that the superior design and quality of Patton product families are your best bet for the 6U Chassis. The following Patton products mate with the 6U chassis.

Model 5406 6U Redundant Backplane/Midplane

The 600 Series chassis is designed to accept Patton's backplane products which can be standard or custom designed per customer specifications. This manual contains a complete description of the Model 5406 Redundant Backplane/Midplane.

Model 5250 Series Power Supply Module

Patton maintains the industry's highest power density footprint. The 3U power supply module provides state-of-the-art N+1 redundant power operation. The Model 5250 Power Supply Module delivers 200 watts in a 3U x 160mm x 8HP CompactPCI format. The 600 Series 6U chassis accepts up to four Model 5250 3U Power Supply Modules.

The Model 5250 is a modular, high power, CPCI plug-in module that supplies standard 3.3V, 5V and 12V DC voltages in a variety of configurations for use in electronic systems. The unit can be operated as either a wide range, AC input or 48V DC input and offers full mechanical compatibility with IEEE-1101.10. Each unit generates full power output with 300LFM (linear feet per minute) airflow. It features the latest CPCI power interface connector, and is fully hot-swappable.

Meets the requirements of: UL, CSA, FCC, NEBS and CE, UL1950, EN 60950, FCC Class B, EN 55022 Class B, NEBS-FR-2063 (1997).

Model 5502 6U Alarm Interface Module

Patton's 6U x 80mm plug-in alarm interface module is designed to monitor and report alarm conditions to a system level controller or a remote alarm panel for high availability/reliability systems.

Inputs to the alarm module come from Patton's redundant power system and the two auxiliary connectors provided on the panel. Both the AUX 1 and AUX 2 connectors provide fully independent and isolated TTL level signals, which can be connected to any external monitoring device you desire.

All inputs can be configured as either Major or Minor alarm events. The Major and Minor Alarms provide a Normally open/Normally closed relay configuration that allows you the flexibility and isolation required to connect to an external controller or an external alarm panel.

This symbol and the CAUTION heading indicates a situation where equipment can be damaged by electrostatic discharge.

The unit is designed to comply with all electrical and mechanical requirements of IEEE 1101.10, UL, CSA, FCC, NEBS, and CE, UL 1950, EN 60950, FCC Class B, EN 55022, NEBS-FR-2063 (1997).

Chapter 3 Installation checklist

Chapter contents

6U quick set-up checklist

The 6U CPCI Model 5406 Backplane/Midplane & Chassis can be easily configured according to your system requirements. Due to the broad application possibilities, the following checklist is provided as a quick set-up guideline.

1. **Select Signaling Environment**—The signaling environment, called the Voltage Input/Output (V(I/O)), can be configured for 3.3V or 5V (factory default) signaling via power bugs, located at the rear, left-side of the backplane (See "Signaling Environment" on page 34).
2. **Connect Frame Ground/Signal Ground (FG/SG)**—You may opt to connect the FG/SG for EMC considerations and noise reduction, via power bugs, located at the rear, right-side of the backplane. The factory default is "no connect" (See figure 17 on page 43).
3. **Assign Shelf Address**—For multi-shelf systems, each sub-rack bus segment can be assigned a shelf address via the S1 header, located at the rear, left-side of the backplane (See "Shelf enumeration bus P4 pins" on page 54).
4. **Install 6U Chassis on Rack**—the chassis front mounting flanges should be securely fastened to the rack with screws.
5. **Install Power Supply Modules**—For N+1 power operation, install up to four Patton power supply modules configured for external DC (or other CPCI compatible power modules) at the front of the chassis.
6. **Install Cards**—Plug the system administration card(s) in the system slot(s) at the front of the 6U chassis, and up to 14 peripheral cards can be plugged into remaining slots. Plug alarm card in the left-hand slot at the back of the chassis, and plug transition cards in remaining slots, if needed.
7. **Wire Rear Panel for Optional VRG/VBAT** (See "Telecom power bus P4 pins" on page 53 and "Telecom ringing bus P4 pins" on page 54.)
8. **Wire Rear Panel for Power** (See "External power connections" on page 42.)

Due to possible injuries to people and severe damage to objects caused by electric shock, always wire for power as the last step.

Chapter 4 System Architecture

Chapter contents

CompactPCI form factor

CompactPCI is flexible in the mechanical and connector area, using a passive backplane and plug-in daughterboards. The architecture is based on the IEC 1101.10 and 1101.11 Eurocard standard for the fixed 160mm depth (for front boards), but allows for two board heights:

- 3U—100mm high
- 6U—233.35mm high

This variety enables a wider variety of applications and industries. 3U, which is the minimum for CompactPCI as it accommodates the full 64-bit CompactPCI bus, is popular for embedded industrial automation applications, while 6U provides additional board real estate for more complex applications. 6U also provides more connectors for rear-panel I/O often needed in telecom products.

Eurocard boards offer a long list of advantages:

✔ Extensive board keying capabilities so that boards can only be plugged into appropriate slots

✔ Card guides for solid rear backplane connectors alignment

✔ Injector/ejector handles

✔ EMC compliance that minimizes electromagnetic interference

To provide maximum configuration flexibility, CompactPCI boards are inserted at the front of the chassis, with options for I/O connections to either the front and/or rear of the card. The cards are firmly held in position by their connector, card guides on both sides, and a face plate which solidly screws into the card cage.

Board front panels

CompactPCI boards provide a front panel interface that is consistent with Eurocard packaging and compliant with IEEE 1101.10 (EMC panels). Ejector/injector handles are used on the boards. 3U boards only use one handle, while the 6U board uses two (see figure 5). Filler panels do not require handles.

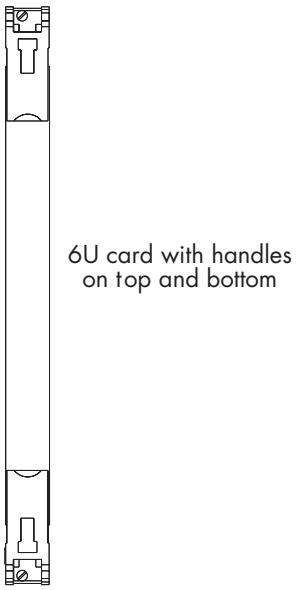


Figure 5. Front panel—6U front-entry card

Transition Boards

There are two types of boards:

- Front-entry boards (described in section “Board front panels”)
- Rear-entry boards for rear-panel I/O

The front-entry boards may route I/O through the backplane. Backplanes that enable rear I/O are called often midplanes because the legs of the backplane connector’s pins stick through the board to become pins for rear-

panel interconnections. An illustration of the front-entry board and rear-panel I/O board interface with the backplane/midplane is shown in figure 6.

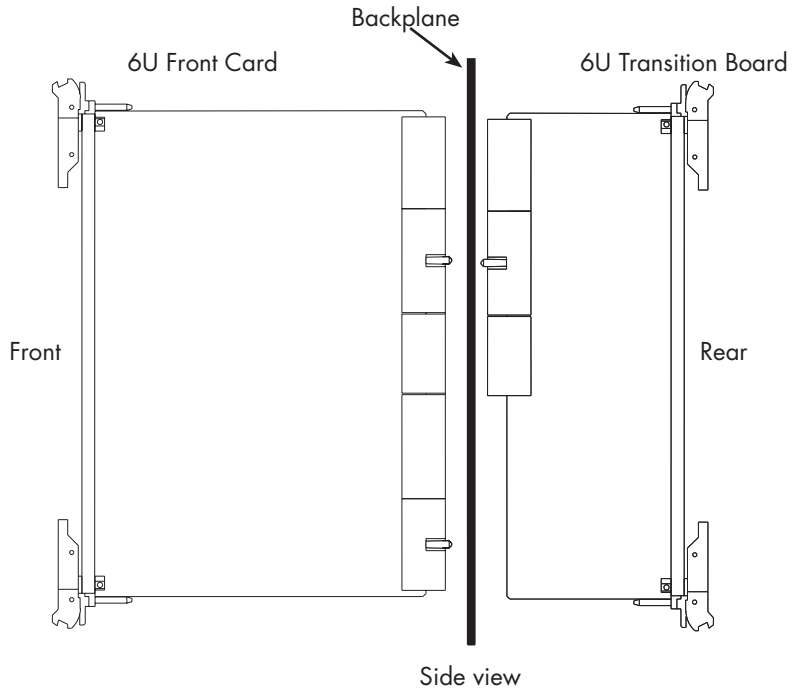


Figure 6. Front/rear boards and backplane interface

Rear-panel I/O boards are 6U in height and are typically 80mm in depth. Other depths are allowed depending on the application requirements. The 6U chassis provides an 80mm transition module section. This section provides seventeen 6U x 80mm slots for an alarm card and/or other CPCI transition modules.

All front-entry board features (handles, keying, alignment pin, EMC, etc.) are also utilized on the rear-entry boards. The rear-panel I/O transition boards are “in-line” with the front-entry boards. This means that the front panels of rear-panel I/O transition boards are reversed (mirrored) from the front boards. The top handles are on the bottom and vice versa. The slot keying holes and hole labels in both the card guides and front panels are upside down compared to the front boards and card guides (see “Keying of CPCI backplanes and boards” on page 48 for more information on keying).

The same connector pin labeling sequence is used on the rear I/O transition boards as on the front boards, with the position numbers going from bottom to top. This is a mirror image of the front board’s layout orientation. Using the same 1-for-1 pin mapping sequence eliminates confusion and I/O signal pin mapping problems. For example, pin A3 is the same on the front boards, on the rear I/O transition board, and on the backplane.

Rear-panel I/O transition boards may have active components in some applications. Power can be applied either through the I/O pins from the front board, or from the normal power and ground pins defined as part of the J1/P1 and J2/P2 connector pin assignments.

Rear I/O transition boards that only populate Rear J5 (RJ5) for the purpose of telephony I/O, must utilize a Type AB connector body on RJ5. This type of connector provides an integral alignment feature that avoids damage to the backplane pins during mating. Patton's 6U Model 5406 Backplane/Midplane complies with this requirement, providing a Type AB connector shroud on RP3, RP4, and RP5.

Pin and socket connectors

The connection between boards and backplane is through a two-piece, 2mm connector. Backplanes use male (pin) connectors and plug-in boards use female (socket) connectors. This pin and socket connector offers greater reliability, particularly when subject to shock, vibration, or temperature variations.

These pin and socket connectors provide:

- Faster propagation times
- Reduced reflection at the bus/connector interface
- Lower noise
- Better impedance matching
- Higher mechanical stability

The connector is a 235-pin device, arranged in 47 rows of 5 pins, with a total of 220 pins (15 pins are lost to the keying area). The connector is shielded and devotes a large number of pins to ground. This reduces reflections, increases EMI immunity in noisy environments, and reduces ground bounce.

The fixed or male connector on the backplane is numbered P1-P5, starting at the bottom. The corresponding female connectors are also numbered from the bottom up as follows:

- 3U cards—J1-J2 (see figure 7 on page 30)
- 6U cards—J1-J5 (see figure 8 on page 30)

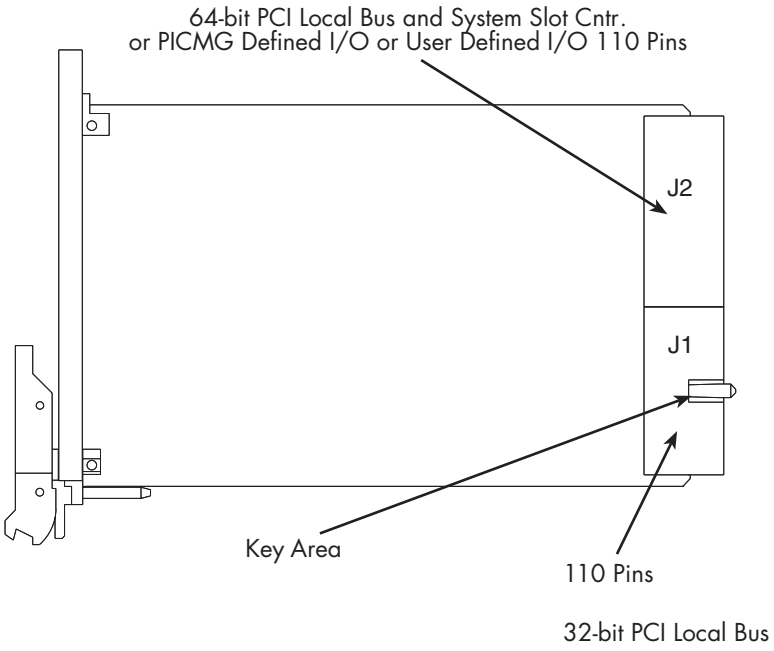


Figure 7. J1 and J2 connectors on the 3U card

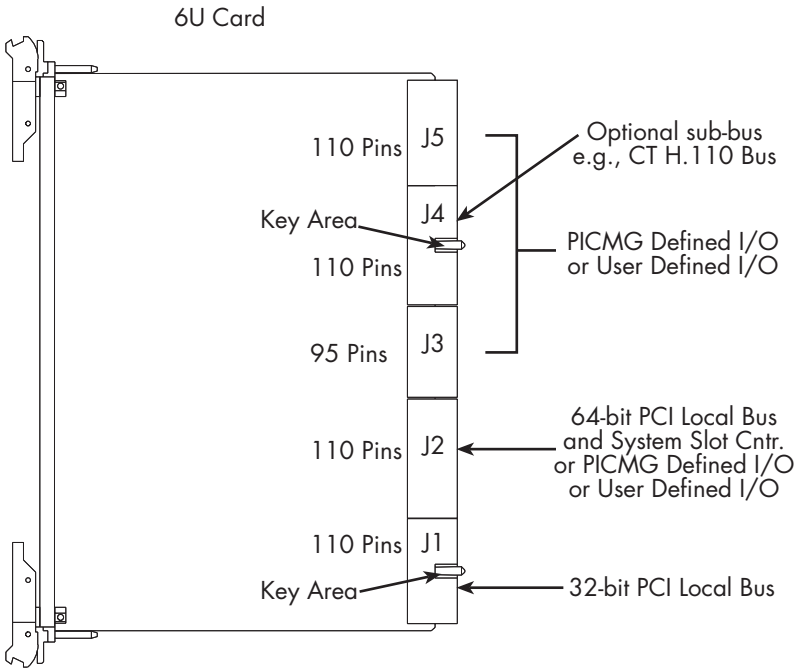


Figure 8. J1 through J5 connectors on the 6U card

3U and 6U cards use a single 220 pin connector for all power, ground, and all 32- and 64-bit PCI signals. This connector consists of two halves—the lower half (110 pins) is called J1/P1 and the upper half (also 110 pins) is called J2/P2. Twenty pins are reserved for future use. The connector is divided in J1/P1, a 25-row connector that includes voltage keying, and J2/P2, a 22-row connector without keying. The 6U card can have up to four additional connectors with a total of 315 pins, which can be used for a variety of purposes.

A system CPU uses J1 and J2, but 32-bit peripherals cards only need to use J1 for full CompactPCI functionality. J3 through J5 on 6U cards can be user-defined I/O. Optional buses, such as the CT H.110 bus, use the J4 position.

J1/P1 & J2/P2 connectors

The CompactPCI bus spans the J1/P1 & J2/P2 connectors, with 32-bit PCI implemented on J1/P1 and full 64-bit PCI implemented on J2/P2 on the 6U Model 5406 Backplane/Midplane. J1/P1 is always devoted to 32-bit PCI in CompactPCI systems, however, use of J2/P2 for 64-bit PCI can be optional. For instance, in a 3U system, J2/P2 may be defined for user I/O, or sub-buses like the CT H.110 bus. J2 is always used on system slot boards to provide arbitration and clock signals for peripheral boards.

Table 5. CompactPCI pinouts on P1/J1 and P2/J2

22	GND	GA4	GA3	GA2	GA1	GA0	GND	P2 /J2 CONNECTOR
21	GND	CLK6	GND	RSV	RSV	RSV	GND	
20	GND	CLK5	GND	RSV	GND	RSV	GND	
19	GND	GND	GND	RSV	RSV	RSV	GND	
18	GND	BRSVP2A18	BRSVP2B18	BRSVPC18	GND	BRSVPE18	GND	
17	GND	BRSVP2A17	GND	PRST#	REQ6#	GNT#6	GND	
16	GND	BRSVP2A16	BRSVP2B16	DEG#	GND	BRSVP2E16	GND	
15	GND	BRSVP2A15	GND	FAL#	REQ5#	GNT5#	GND	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND	
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND	
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND	
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND	
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND	
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND	
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND	
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND	
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND	
5	GND	C/BE[5]#	GND	V(I/O)	C/BE[4]#	PAR64	GND	
4	GND	V(I/O)	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND	
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND	
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND	
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND	

Table 5. CompactPCI pinouts on P1/J1 and P2/J2 (Continued)

25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	P1/J1 CONNECTOR
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND	
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND	
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	SDONE	SBO#	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND	
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND	
12-14	Key Area							
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	
9	GND	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND	
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND	
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	
4	GND	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	Z	A	B	C	D	E	F	

J3/P3 through J5/P5 connector

J3/P3 through J5/P5 connectors, available only in 6U systems, are generally defined for user I/O. However, sub-bus interconnects (for example, CT H.110 bus) can be configured on the J4/P4 connector.

Reserved Pins

There are bused and non-bused reserved pins as noted below:

- The BRSVPxxx signals SHALL be bused between connectors and are reserved for future CompactPCI definition.
- The RSV signals are non-bused signals that SHALL be reserved for future CompactPCI definition.

Power Pins

The 6U Model 5406 Backplane/Midplane signaling environment is factory-defaulted at 5V. However, it has a customer-selectable option to change it to 3.3V by changing the jumper on the power bugs located at the back of the backplane (see “Signaling Environment” on page 34). All connectors on Patton’s 6U Model 5406 Backplane/Midplane provide pins for +5V, +3.3V, +12V and -12V operating power.

In addition, there are power pins labeled +V(I/O). The V(I/O) power pins on the connector are used to power the buffers on the peripheral boards, allowing a card to be designed to work in either interface. CompactPCI supports this dual-interface scheme by utilizing backplane connector keying (see “Keying of CPCI backplanes and boards” on page 48 for more information).

Backplane Architecture

The Model 5406 Backplane/Midplane provides two electrically separate, CompactPCI bus segments. Each CPCI bus segment is composed of eight 6U board locations (at 33 MHz) with 20.32 mm (0.8 inch) board center-to-center spacing.

There are also four 47-socket Positronics power connectors, two on the left and two on the right, to mount Patton’s Power Supply Modules (3U x 160mm) —configured for external DC input—or other CPCI compatible power modules. The connectors meet requirements specified in the *PICMG 2.11, R1.0 CompactPCI Power Interface Specification*. Refer to “In-rack power connections” on page 44 for a description of these features.

The front view of the 6U Model 5406 Backplane/Midplane is shown in figure 9.

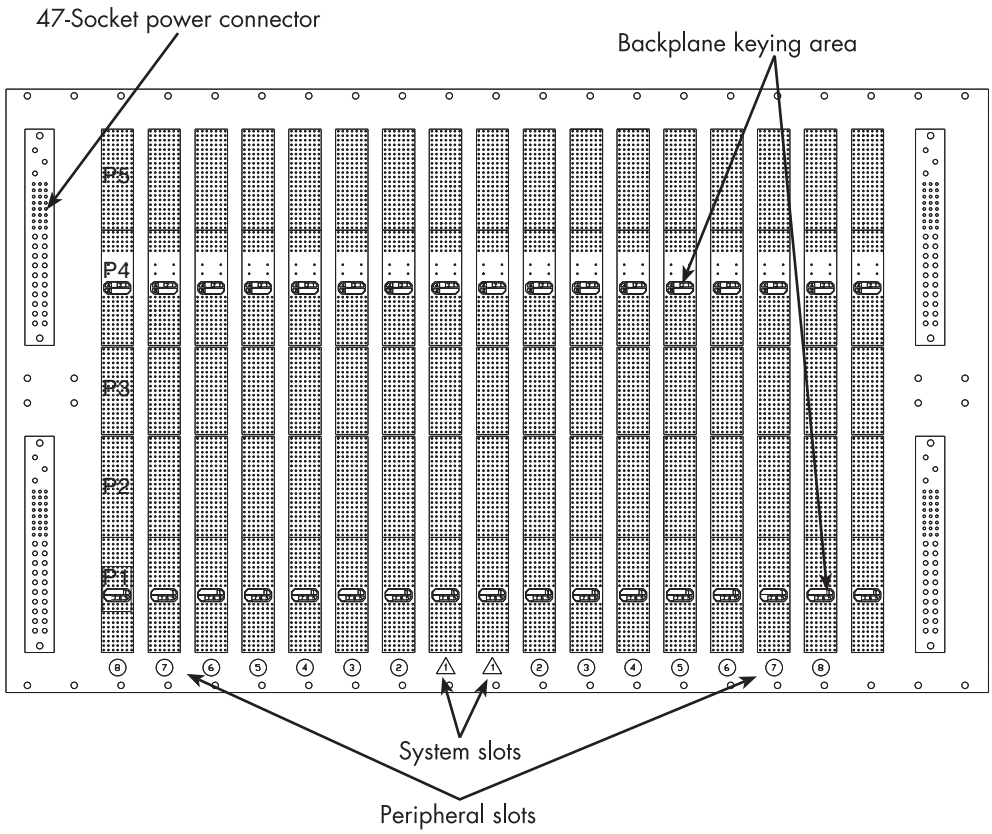


Figure 9. Front view of backplane

Signaling Environment

The 6U Model 5406 Backplane/Midplane provides for either a 5V or 3.3V signaling environment.

PCI allows for two types of buffer interfaces for interboard connection. The V(I/O) power pins on the connector are used to power the buffers on the peripheral boards, allowing a card to be designed to work in either interface. These are called universal boards. It should be noted, that backplanes are never universal. The V(I/O) level distributed on the backplane is either 5.0V or 3.3V. It is only possible that boards can be tolerant of either voltage levels, and considered universal.

The factory default setting for the 6U Model 5406 Backplane/Midplane is for the 5V signaling environment (denoted by the brilliant blue connector key). The signaling environment (denoted by the cadmium yellow connector key), called the Voltage Input/Output (V(I/O)), can be configured for 3.3v signaling via a power bug located at the back of the backplane.

Changing the signaling environment voltage

The following outlines the steps to change the default setting of 5V to 3.3V.

Due to a safety hazard, only rewire the signaling environment prior to wiring the board with external power connections.

1. Using a flat-head screwdriver, remove the four screws (two on top, two on bottom) on the left, rear panel of the chassis (see figure 10).

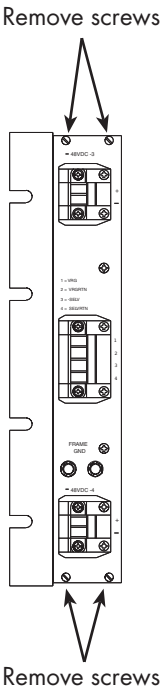


Figure 10. Removing left rear panel of chassis

2. Using a phillips screwdriver, remove the screw and wire from the 5V ring terminal (labeled J16) (see figure 11). Do not remove the wire from the V(I/O) terminal (labeled J17).

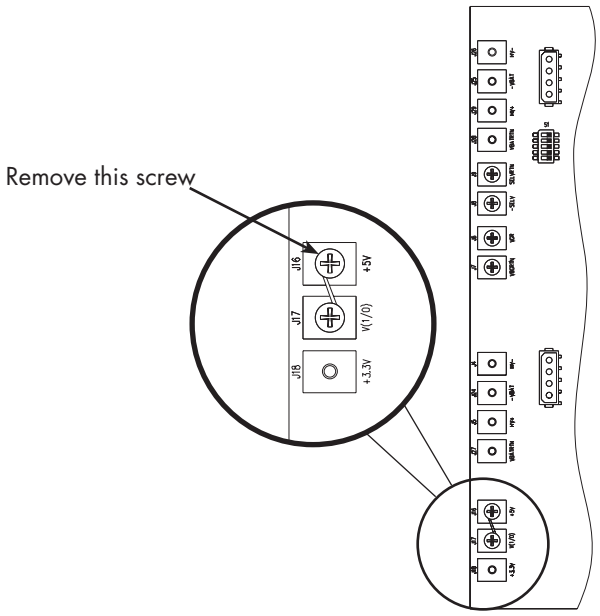


Figure 11. Removing 5V ring terminal screw and wire

3. Keeping the wire connected to the V(I/O) terminal, connect the other end of the wire to the +3.3V terminal (labeled J18), securing the screw in the ring terminal with a phillips screwdriver (see figure 12).

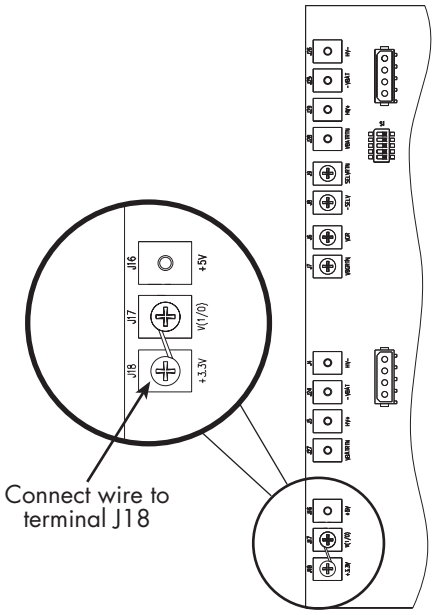


Figure 12. Connecting 3.3V ring terminal screw and wire

CAUTION

To avoid equipment damage, after you change the V(I/O) to 3.3V, replace the blue connector key with the cadmium yellow connector key. See "Keying of CPCI backplanes and boards" on page 48 for more information on keying.

Slot Designation

Consistent with CompactPCI specifications, the CPCI bus segment consists of one system slot, and seven peripheral slots. The system slot is denoted with a "triangle" compatibility glyph, and the seven peripheral slots are marked with a "circle". The 6U CPCI Model 5406 backplane/midplane has two, electrically separate CPCI bus segments. In CPCI bus segment one, the system slot is on the right, and in CPCI bus segment two (see figure 12), the system slot is on the left (see also figure 9 on page 33, which shows both bus segments together).

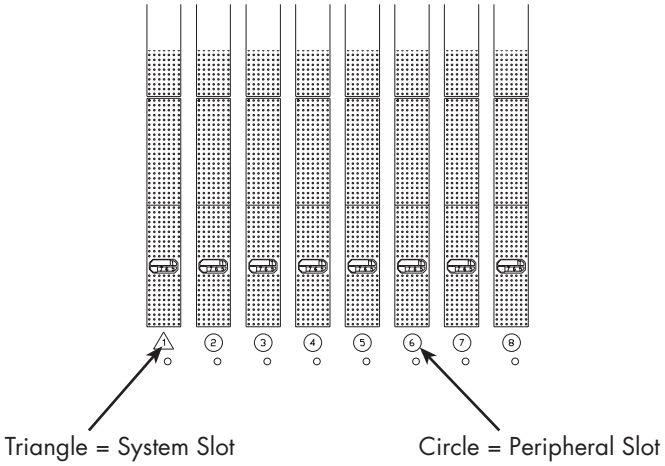


Figure 13. Slot compatibility glyphs (segment 2 shown)

The system slot provides arbitration, clock distribution, and reset functions for all boards on the segment. The system slot performs system initialization by managing each local board's IDSEL signal. The peripheral slots may contain simple boards, intelligent slaves, or PCI bus masters.

CompactPCI defines slot numbering based on the concept of physical and logical slots. Physical backplane slots are designated 1, 2, 3, through N, where N is the number of slots. Physical slot numbering starts at the left on the 6U Model 5406 Backplane/Midplane (see figure 14).

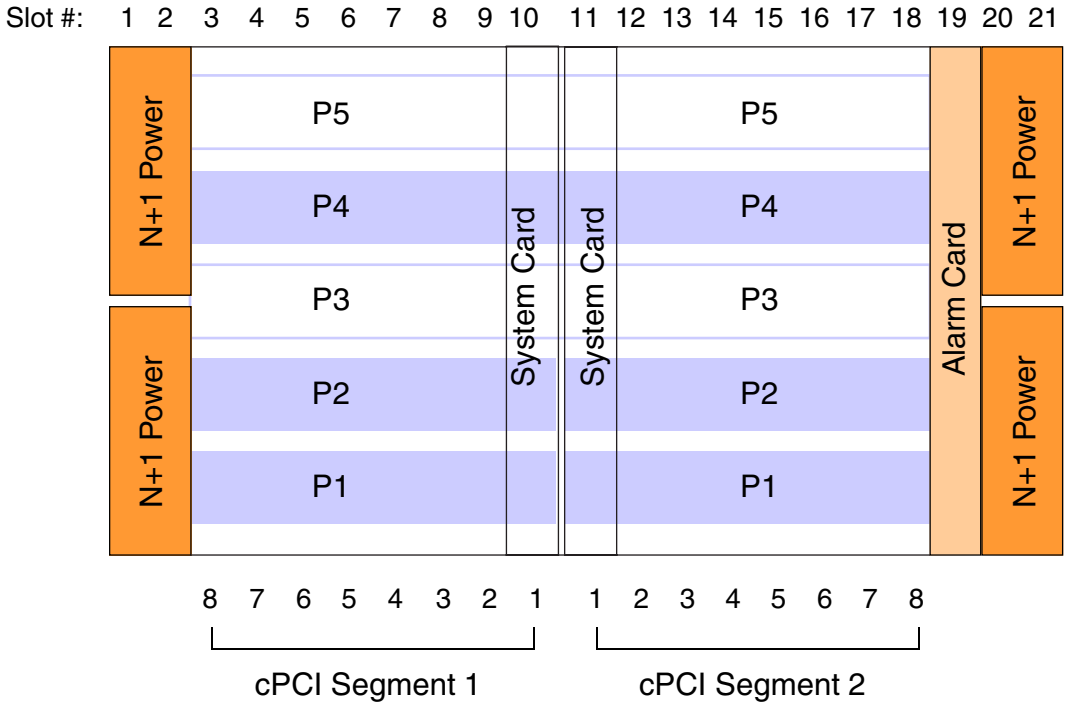


Figure 14. 6U backplane configuration

Logical slot numbers are defined by the IDSEL signal and associated address used to select the slot. Logical numbers are used in the nomenclature to define the physical outline of a connector on a bus segment. Logical and physical slot numbers may not always coincide.

Each slot may be implemented with 1 to 5 connectors numbered P1–P5, starting from the bottom of the board.

Bus segments

The 6U Model 5406 Backplane/Midplane is configured for 64-bit/32-bit interoperability. For example, a 32-bit processor and peripherals can be plugged into a 64-bit backplane. Because the backplane is passive, it is possible to have a 32-bit CPU in a system working with 64-bit peripherals.

The system slot uses J1/P1 and J2/P2 to allow the arbitration and clock signals to be connected to the backplane from the system slot board. Connectors on the backplane utilize pin staging to enable hot swapping of boards. (See Hot-Swap Capability on page 52 for more information.)

The CompactPCI bus segment on the 6U Model 5406 Backplane/Midplane bus all signals in all slots within the segment except the slot specific signals: CLK; REQ#; and GNT#. Each logical slot also has a unique IDSEL signal connected to one of the upper ADxx signals for configuration (plug and play) decoding. The 6U Model 5406 Backplane/Midplane implements the modular power supply connector that provides connection

for the power supply signals DEG# and FAL# at the system slot. (See table 6 for more information on the backplane signals.)

Backplane signals

CompactPCI utilizes PCI signals as defined by the PCI Local Bus Specification, with some additional signals. The additional signals enhance system operation, and do not affect the PCI signals. See table 6 for a list of the backplane signals with a brief description.

Note See PICMG, 2.0, R2.1 CompactPCI, Specification for more information.

Table 6. Backplane signals

Signal	Description
CLK0—CLK4	Backplane clock routing supports CLK0-CLK4. CLK5-CLK6 provided by the system slot board are not routed on the backplane.
IDSEL	The PCI signal IDSEL is used to provide unique access to each logical slot for configuration purposes. The backplane makes the connection to IDSEL at each logical slot's connector with minimum trace length.
REQ#/GNT#	Request/grant signals. the system slot on the backplane supports the full complement of REQ#/GNT# signals.
PRST#	Push button reset—an active low true TTL signal generated by a switch closure or an open-collector driver. It is used to reset the system slot board, which in turn would reset the rest of the system using the PCI RST# signal.
DEG#/FAL#	Power supply status. • DEG#—derating signal—an output from the power supply to indicate that the supply is beginning to derate its power output. • FAL#—supply fail signal—an output from the power supply to indicate that it has failed.
SYSEN#	System slot identification—this pin is grounded on the backplane at the system slot so the board may identify installation into the system slot. This pin is not connected on the backplane for the remaining slots.
ENUM#	system enumeration—this low true TTL open-collector signal is driven by hot swap compatible boards after insertion and prior to removal. the system master uses this interrupt signal to force software to interrogate all boards within the system for resource allocation regarding I/O, memory, and interrupt usage.
GA0/GA4	Geographic addressing –the GA0-4 signals are available on the top five pins of the J2/P2 connector on backplanes that implement 64-bit. 32- and 64-bit boards use it to provide a unique differentiation based upon which physical slot the board has been inserted.
INTA# -INTD#	PCI interrupt binding of the BIOS setup program require backplane assignments from the system slot interrupt pins INTA#—INTD# to the logical board slot interrupts. Refer to the "CompactPCI Specification", PICMG 2.0, R2.1 for backplane assignments.
INTP -INTS	Legacy IDE interrupt support—two additional non-PCI interrupts are defined for IDE boards. These signals are active high TTL level signals and do not have to meet the PCI electrical buffer characteristics. They are provided to ease the transition from compatibility mode to native mode PCI IDE operation.

Alarms

In CompactPCI, systems the Alarm Card is designed to monitor and report alarm conditions to a system level controller or a remote alarm panel. The connections from the Alarm Card to the system level controller are passed through the connector. No backplane routing is required. However, backplane routing may be required for routing external sensors to the Alarm Card. This is called a Subrack Alarm Bus. The 6U Backplane/Midplane provides this type of Subrack Alarm Bus.

Five signals (AI1-AI5) from the 6U backplane are entered from the P3 connector to the Alarm Card. The possible monitoring conditions are:

- Airflow sensor
- Temperature sensor in fan tray
- Watchdog on Voice Cards (CT Bus)
- Watchdog on Switch Cards (CT Bus)
- Watchdog on Admin Card

The five alarm signals from the backplane can be configured using Patton's Model 5502 Alarm Module, to output as Major or Minor Alarms. Furthermore, the alarm outputs can be configured with time-outs from 1-9 minutes. (See "Model 5502 6U Alarm Interface Module" on page 22 for more information.)

Patton can customize the internal alarm signals per customer requirements. Or, backplanes can be customized to disconnect the alarm bus signals from P3. When disconnected, P3 is then standard I/O.

The Backplane Alarm wiring is shown in figure 15 on page 40.

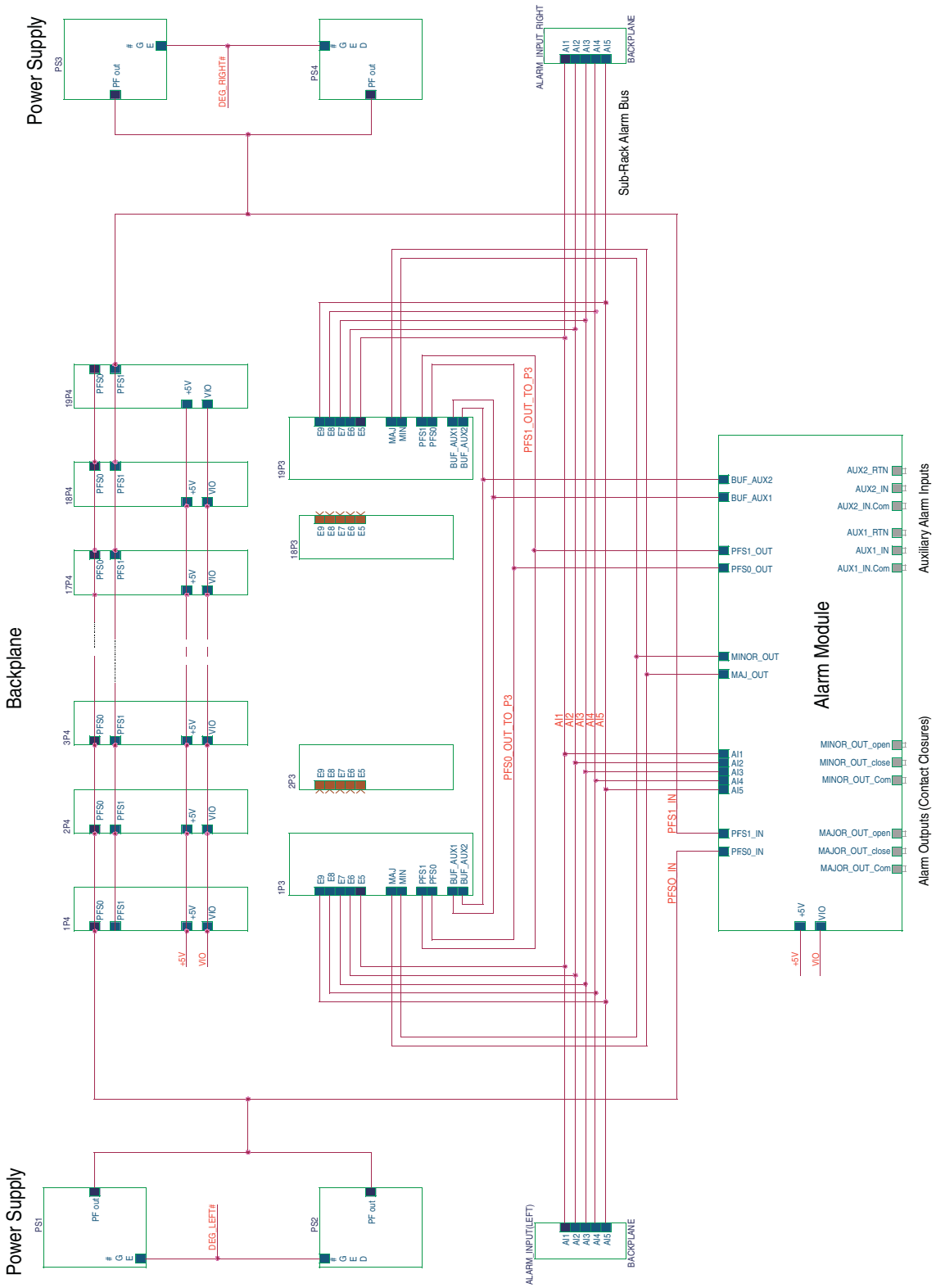


Figure 15. Backplane alarm wiring detail

Backplane power distribution

Power is distributed in a CompactPCI system via the backplane. The backplane provides standard direct current (DC) supply voltages as specified in table 7 below

Table 7. Power specifications

Mnemonic	Description	Nominal Value	Tolerance	Max. Ripple
5V	+5VDC	5.0V	±5%	50 MV[a]
3.3V	+3.3VDC	3.3V	±5%	50 MV[a]
+12V	+12VDC	12.0V	±5%	50 MV[a]
-12V	-12VDC	-12.0V	±5%	50 MV[a]
GND	GROUND			

a. Maximum ripple is very difficult to accurately measure and therefore requires good measurement techniques. Measurement should be made at full load at 20 MHz bandwidth with a 22mF capacitor located at the measurement point.

The Model 5406 Backplane/Midplane & Chassis provides two types of power connections for N+1 power operation:

- External power connections
- In-rack power connections

External power connections

The chassis provides a rear DC interface panel with -48V DC power interfaces for N+1 power operation and dual ground bugs, as shown in figure 16 below. The connectors are described in table 8.

Figure 16. Power terminals on 6U rear DC interface panel

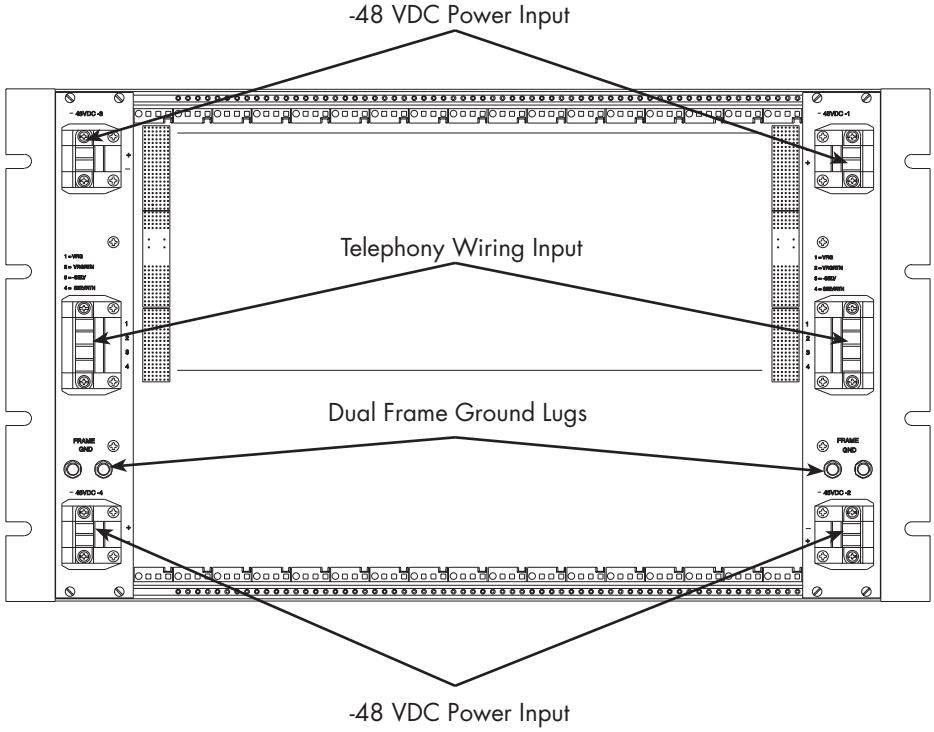


Table 8. Description of rear interface panel connectors

Item	Description
-48 VDC power terminal	DC rear-entry module accepts 36 VDC–72 VDC @ 10 Amp max input via Phoenix connector. Polarity should be applied as marked (negative—top position, positive—bottom position). Each connector is independent and designed to power one 3U power supply module. there are four connectors provided for n+1 power operation.
VRG	Telecom power source—the VRG and VRGRTN contacts connect a ring voltage source, such as a central office ring signal to the backplane. This is typically 60VRMS—170VRMS, 16HZ to 72HZ.
VRGRTN	Telecom power source return
-SEL VBAT	Safety extra low voltage or “short loop” battery (voltage within SELV limits) the –SEL VBAT and SEL VBAT RTN connectors connect an isolated power source to the backplane for use in powering telephony lines. They are not intended to power the 3U power supplies.
SEL VBAT RTN	Short loop battery return (voltage within SELV limits)

Table 8. Description of rear interface panel connectors (Continued)

Item	Description
Ground bugs	The dual-frame ground bugs must be used to connect the chassis to earth ground on dc interfaces. Failure to do this will cause excessive RF emissions and could possibly create a safety hazard. The double ground bug meets nebs and will accept AMP part# 606209-1. NEBS requires a double bug on DC chassis to ensure that the ground connection will not rotate and become loose.

The dual frame ground lugs on DC interfaces must be used to connect the chassis to earth ground. Failure to do this will cause excessive RF emissions and could possibly create a safety hazard.

Backplane power bugs and connectors

The 6U transition module provides phoenix connectors for the –48V DC power interfaces, discussed in the previous section (figure 16 on page 42). However, if you purchased the 6U Model 5406 Backplane/Midplane without the chassis, there are different styles of connectors (figure 17).

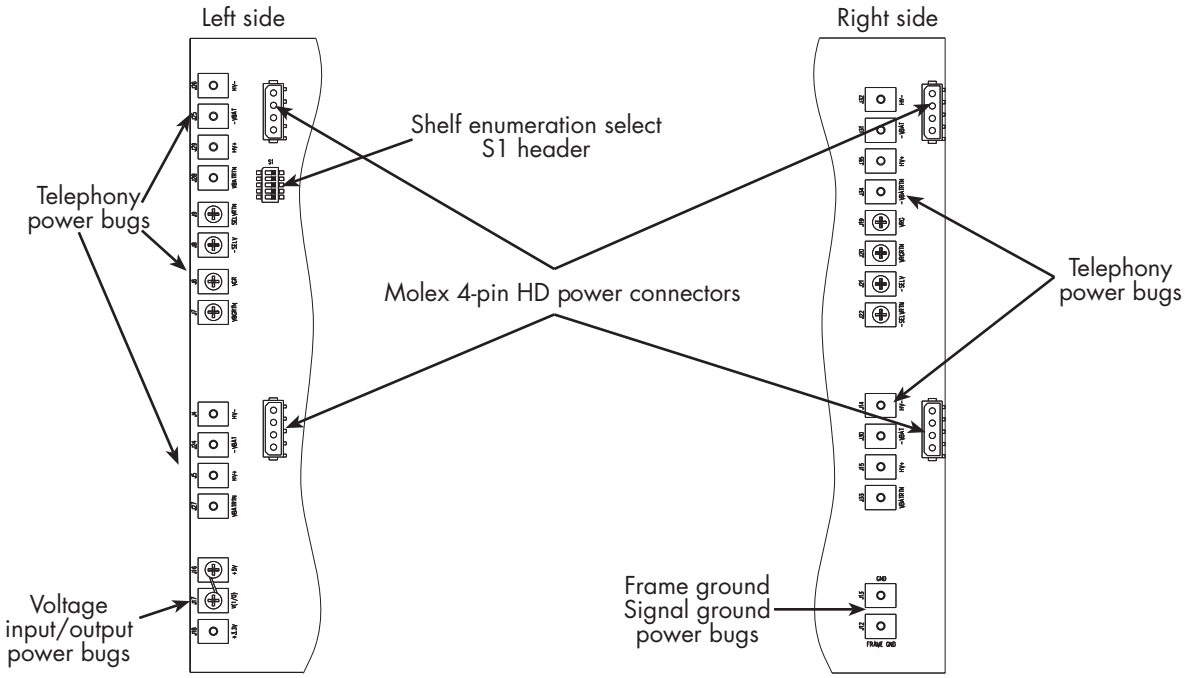


Figure 17. Internal backplane power bugs and connectors

Table 5 provides a description of the internal backplane connectors shown in Figure 13 above.

Table 9. Description of internal backplane connectors

Item	Description
P1—P4	DC rear-entry module accepts 36 VDC–72 VDC @ 10 Amp max input via molex 4-pin connectors. polarity should be applied as marked. the male (pin) connector is on the backplane, and the mate is the female (socket) connector. each connector is independent and designed to power one 3U power supply module. there are four connectors provided for N+1 power operation.
J4–J9, J14, J15, J19–J22, J24–J35	• No. 6 X 3/8 in. screw-ring terminal power bugs that you hard-wire. ± HV (high voltage) requires 14 GA wire. • Refer to Table 8 on page 42 for descriptions of VRG (J1), VRGRTN (J2), -SEL VBAT(J3) and SEL VBATRTN (J4). • -VBAT (J5)—Telecom power source • VBATRTN (J6)—Telecom power source return
J12—J13	No. 6 X 3/8 in. screw-ring terminal power bugs that you hard-wire. Depending on the environment, J12—frame ground (FG) and J13—signal ground (SG) and can be wired together for EMC considerations and noise reduction. (See also "Electromagnetic compatibility (EMC)" on page 18)
J16-J18	No. 6 X 3/8 in. screw-ring terminal power bugs that you hard-wire to change the voltage input/output From 5V (factory default) to +3.3v. (See "Signaling Environment" on page 34)
S1	Rocker switches to assign the shelf address (see "Shelf enumeration bus P4 pins" on page 54).

The –Vbat and VbatRtn telecom power supply buses are qualified to source Unearthed SECONDARY HAZARDOUS voltages as defined by IEC950 and harmonized derivative specifications. The –SELVbat and SELVbatRtn buses are not qualified for SECONDARY HAZARDOUS voltage distribution. Voltage sourced on the –SELVbat bus is within SELV limits.

In-rack power connections

Four Positronics 47-pin/socket connectors are provided for in-rack modular power supplies on the 6U Model 5406 Backplane/Midplane for N+1 power operation (See figure 9 on page 33). The female connector is located on the backplane and the male connector is located on the power supply module.

The power connectors mate with Patton's 3U Power Supply Module. In the 6U chassis, there is room for four power supply modules, 3U high x 160mm deep x 8HP wide.

Note The chassis guide rails are 1/2HP offset for plug-able power supplies. That is to say, the card guide's slot and injector/ejector PCB mounting surface are shifted 0.1 inch to the right of the card. The power supply card guide is green in color.

The backplane power connector pin assignments are provided in table 10. Please note that some functions are not currently available on the 6U Model 5406 Backplane/Midplane. The excluded functions are footnoted with a (1).

Table 10. Backplane power connector pin assignments

Pin no.	Staging	Signal Name	Description
1-4	M	V1	+5 VOLT OUT
5-12	M	RTN	SIGNAL GROUND
13-18	M	V2	+3.3 VOLT OUT
19	M	RTN	SIGNAL GROUND
20	M	V3	+12 VOLT OUT
21	S	V4	-12 VOLT OUT
22	M	RTN	SIGNAL GROUND
23	M	RES	RESERVED
24	S	RTN	SIGNAL GROUND
25	M	ADD1	ADDRESS BIT 1[a]
26	M	RES	RESERVED
27	S	EN#	ENABLE SIGNAL—0 will enable the supply
28	M	ADD2	ADDRESS BIT 2[a]
29	M	V1 ADJ	V1 ADJUST[a]
30	M	V1 SENSE	+5 VOLT SENSE
31	M	ADD3	ADDRESS BIT 3[a]
32	M	V2 ADJ	V2 ADJUST[a]
33	M	V2 SENSE	+3.3 VOLT SENSE
34	M	S RTN	SIGNAL GROUND
35	M	V1 SHARE	+5 VOLT CURRENT SHARE—connect between modules
36	M	V3 SENSE	+12 VOLT SENSE[a]
37	M	TX	SERIAL COMM, TRANSMIT[a]
38	M	DEG#	DEGRADE SIGNAL—0 indicates imminent failure
39	M	INH#	INHIBIT SIGNAL[a]
40	M	RX	SERIAL COMM, RECEIVE[a]
41	M	V2 SHARE	+3.3 VOLT SHARE—connect between modules
42	M	FAL#	FAIL SIGNAL—0 indicates module has failed
43	M	INT	SERIAL COMM, INTERRUPT[a]
44	M	V3 SHARE	V3 SHARE[a]
45	L	CGND	CHASSIS GROUND
46	S	ACN/+DC IN	POSITIVE DC VOLTAGE INPUT
47	S	ACL/-DC IN	NEGATIVE DC VOLTAGE INPUT

a. This function is not provided on the 6U Model 5406 Backplane/Midplane. It is listed in the table as an optional CompactPCI specification. In other words, Patton can customize the backplane connectors to make the function available at that pin location, if so required.

Front panel keying for power supplies

Power supply keying options have been registered with PICMG. Since power supplies use a different type of connector than other CompactPCI slots, there is no possibility of mating problems with 2mm connectors. The power supply key options are independent of the 2mm application card keys, and may duplicate key codes that are used for different purposes elsewhere in the system (see "Keying of CPCI backplanes and boards" on page 48 for more information on front panel keying).

Specific front panel keying is defined to prevent damaging an AC power supply inserted into a backplane wired for DC and visa versa.

Note Refer to the *PICMG 2.11, R1.0 CompactPCI Power Interface Specification* for more information on keying

Power decoupling

CompactPCI boards can use any of the voltages in Table 7 on page 41. Adequate power decoupling is required on the backplane for 5V and 3.3V power to ensure power operation will not be intermittent. Power voltages on the backplane are decoupled to ground so as to provide for reasonable management of switching currents (DI/DT). Low-impedance power planes and connections to low equivalent series resistance (ESR) capacitors are used. The bypass guidelines that are used for each connector are provided in table 11.

Table 11. Backplane decoupling specifications

Mnemonic	Description	Decoupling Capacitance	Voltage[a]
5V	+5 VDC	44 mF ±20%[b]	15 V MIN.
3.3V	+3.3 VDC	44 mF ±20%[b]	10 V MIN.
V(I/O)	+5/3.3 VDC	44 mF ±20%[b]	15 V MIN.
+12V	+12 VDC	15 mF ±20%	36 V MIN.
-12V	-12 VDC	15 mF ±20%	36 V MIN.

a. Voltage values are three times the decoupled voltage value to avoid stressing a tantalum capacitor due to very fast power supply turn-on times.
b. Recommended decoupling capacitance per connector best distributed across the length of each connector.

Hot-Swap Capability

Hot-swapping is the capability of removing and replacing components without turning off the system. Hot-swap capability is becoming increasingly important in systems requiring continuous operation at some level. Because boot times of many popular operating systems are long, the hot-swap capability is crucial for high-end PC servers, and even more so for telecommunication systems, such as base stations, where board-level exchanges must be made without any downtime. CompactPCI supports dynamic configuration to allow hot

removal/insertion of boards without interrupting backplane transactions or disturbing DC voltages in the power system.

The hot-swap feature is implemented on the CPCI boards, not on the backplane. The backplane remains passive. Therefore, CompactPCI boards either are or are not hot-swappable.

Signal lines must be precharged to 1V before being plugged into the backplane to maintain ongoing bus transactions. Also, power must be ramped up or down in a controlled manner to allow the power supply to adjust to the change in load. The power supply, ground and signal pins on the connectors are staged to allow sequencing, so as to not disturb the operation of the surrounding boards in the bus. The three levels of sequencing are:

- Short pins for BD_SEL#
- Medium pins for signals
- Long pins for power/ground

The system uses two levels of sequencing so that power/ground is made first/broken last. The short pin (BD_SEL#) connection is made only when the board is firmly seated, which signals the control circuitry to power up any high-current devices. Conversely, BD_SEL# breaks first to provide early warning to the control circuitry.

The three levels of hot-swap capability, which involves the degree of user intervention required for hot-swapping are defined in table 12.

Table 12. Hot-swap form factors

Type	Requirements	Hardware Connection	Software Connection
Basic hot-swap	Stages power pins—bus isolation control—Power-Amp circuitry—separate clock line for each slot	Manual	Manual
Full hot-swap	Basic features, plus ENUM line—injector/ejector switch—front panel LED—software monitoring and control	Manual	Automatic
High availability	Full features, plus hot-swap controller	Automatic (hot spares)	Automatic

Hot-Swap Insertion Sequence

The sequencing for hot-swap insertion of boards is as follows:

1. Physical insertion of board begins.
2. Long pins (power) make contact. Signals begin to enter conditioned (precharged) state.
3. All signals are precharged.
4. Medium (signal) pins make contact.
5. Power up and insertion complete.

Hot-swap removal sequence

The sequencing for hot-swap removal of boards is as follows:

1. Physical extraction of board begins.

2. Short pin (BD_SEL#) breaks contact. All signals begin to enter conditioned state. Power down sequence begins in back end circuitry.
3. All signals are conditioned.
4. Medium pin (signals) break contact.
5. Power down and extraction complete.

Keying of CPCI backplanes and boards

To safely support overlapping uses of CompactPCI user-definable pins, keying mechanisms are required. The two types of keying mechanisms are:

- Backplane connector keys—defined in IEC 61076-4-101
- Front panel and cardguide keys—defined in IEEE 1101.10

Assignment and registry of these keys is centrally administered by the PICMG Technical/Executive Committee.

Backplane connector keys

Backplane connector keys prevent inadvertent installation of boards designed for one particular purpose into backplane slots defined for another.

The Type A connectors used in the J1/P1 and J4/P4 locations allow installation of a keying block having eight coding positions. Within the keying block, four coding positions are filled with blocking pins and four are left open to receive pins from the mating keying block. There are 70 mutually exclusive mating pairs.

Note Refer to Annex D of IEC 61076-4-101 for summary

There are currently ten defined backplane connector keys, four of which (brilliant blue, cadmium yellow, nut brown and strawberry red) are discussed below.

The 6U Model 5406 Backplane/Midplane is available in either conventional 5.0V logic or 3.3V (See “Signaling Environment” on page 34). To prevent damage to the system resulting from incorrect insertion of cards with differing logic, coding keys are snapped into the male (backplane) and female (card) connectors. Positions 12–14 of the J1/P1 connector are used for the voltage keying mechanism. The unique, bright color of the coding pairs allows for quick and easy visual identification and differentiation. The mechanical design ensures electrical contact will not take place in the event the wrong board is inserted into a coded slot.

Note Refer to *“Keying of CompactPCI Boards and Backplanes”, PICMG 2.10, R1.0* for more information

A brilliant blue connector key (RAL #5007) is used to denote 5.0V logic, and cadmium yellow (RAL #1021) for the 3.3V logic. Universal boards may operate in either 5.0V or 3.3V systems. Typically, universal boards are

shipped with a 5 volt key installed, and a spare 3.3 volt key, with a recommendation to the user to install the key which matches the system. In some cases, universal boards may not have any keying.

The V(I/O) level distributed on the backplane can be either 3.3V (cadmium yellow key) or 5.0V (brilliant blue key). Backplanes are never universal. It is only possible that boards can be tolerant of either voltage levels, and considered "universal".

The J4/P4 backplane connector key, when populated, will have a key signifying which bused interconnect is in use, or if the connector is allocated for user I/O, indicated by the nut brown key. A strawberry red coding key, RAL #3018, is used exclusively for the CT H.110 bus interconnect on J4/P4. Telephony cards would use the corresponding strawberry red coding key. This prevents the use of non-telephony boards with alternate J4 definitions from being used in the backplane. However, other boards not using the J4 connector may still be used.

If you have purchased Patton's 6U Model 5406 Backplane/Midplane with the H.110 bus configured on P4, you MUST use a processor that is H.110 compliant, or remove the J4 connector from the processor card. Failure to do so will result in damage to the processor card and the backplane.

Front panel and cardguide keys

Keying to functionally identify connectors J2, J3, and J5 is located at the board front panel-to-card guide interface. They are called Front Panel Keys, pursuant to IEEE 1101.10.

The card guides, located on the chassis, and the card's handles have three rectangular cavities (along with an alignment pin on the card, and alignment pin chamber on the card guide. (See also "Electrostatic discharge (ESD) protection" on page 19). Three keying pegs can be inserted, which fill half of the cavity in any of four possible orientations. The mating key block on the card handle is fitted with keying pegs in complimentary orientation to the card guide keys.

Note Refer to *"Keying of CompactPCI Boards and Backplanes", PICMG 2.10, R1.0* for more information.

The three top cavities (6U cards only) are labeled A, B, C, and the three bottom cavities are D, E, and F. The cavities are hierarchically arranged, with cavity D on the lower keying block being the major functional designator. Cavity E provides additional functional detail, and cavity F provides slot specific I/O differentiation. The keying cavities in the lower key block differentiate the utilization of J2 for 3U boards, and may also be used with upper key blocks of 6U boards to differentiate uses of J3 and J5.

3U cards use just the lower keying block (cavities D, E and F), since there is only one handle. This results in 64 keying possibilities for the 3U form factor. A 6U card has two handles, so it uses both the top and bottom keying blocks (A-F), resulting in 4096 keying possibilities.

Keying pegs come in two colors: red and grey. The red keying pegs are always used for controller system cards/slots, and the grey pegs are used for peripheral cards/slots.

The majority of the 4096 available keying combinations are primarily used for differentiation of slot specific, user-defined I/O functions. Only those keying combinations needed to protect bused interconnects on J2/P2, J3/P3, and/or J5/P5 will be reserved. The PICMG registry, now under development, will enable companies to identify their keying scheme and prevent other companies from using the same scheme.

Due to dangerous Telephone Network Voltages (TNV), four, unique front panel keys used exclusively for the CT H.110 Bus are required.

If your 6U model has the CT H.110 bus interconnect on the J4/P4 pins (identified with the strawberry red connector key), there are four reserved front panel keys, reserved for exclusive use due to dangerous telephone network voltages (TNV).

To prevent damaging an AC power supply inserted into a backplane wired for DC, and to avoid damaging a DC power supply inserted into a backplane wired for AC, specific front panel keying for plug-in power supplies is defined. See “Front panel keying for power supplies” on page 46.

Chapter 5 CT H.110 Bus Architecture

Chapter contents

CT H.110 Bus

The CompactPCI Computer Telephony (CT) Specification extends the capabilities of the CompactPCI architecture to support specific application needs within the telecom industry, as follows:

- ✔ Hot-swappable Time Division Multiplexed (TDM) bus on J4/P4 complying with the *Enterprise Computer Telephony Forum (ECTF) H.110* specification
- ✔ Two-wire and four-wire I/O on J5/P5 for analog and digital telephony
- ✔ 48 volts DC and ringing distribution
- ✔ Frame-grounding techniques based on IEEE 1101.11
- ✔ Sub-bus and front-panel keying
- ✔ Geographical slot addressing and shelf enumeration

If you have purchased the 6U Model 5406 Backplane/Midplane with the H.110 bus configured on P4, you MUST use a processor that is H.110 compliant, or remove the J4 connector from the processor card. Failure to do so will result in damage to the processor card and the backplane.

A dual-bus architecture is the most effective way to handle voice data streams as well as supervisory and control messaging. This dual architecture is provided with:

- An H.110 bus for the voice data streams, and
- A CompactPCI bus for the supervisory and control messaging.

The CT H.110 bus carries TDM streams, which are time-slotted to carry multiple voice channels. For example, a T1 stream would consist of consecutive frames that each have 24 slots for the interleaving of samples from 24 voice channels.

The CT H.110 bus can carry a TDM stream of 4096 voice-grade channels, each of which represents a 64-kbit/sec. (8 kbyte/sec.) data stream. This considerably reduces the traffic that would otherwise need to be routed over the CompactPCI bus.

The CompactPCI bus supports command/monitoring and system initialization, providing:

- 133 Mbyte/sec. peak data transfer rates
- hot swap capability
- low system-level cost
- Windows NT-friendly hardware

In addition the backplane passthrough, called a midplane, connector on J5 provides:

- Telecom I/O, such as T1/E1
- User I/O, such as Ethernet, Fiber Channel, and so on.

H.110 TDM bus P4 pins

The following pins implement the ECTF H.110 (CT bus) on P4. Unless otherwise specified below, all H.110 pins are of medium (level 2) length.

Table 13. Description of H.110 TDM bus pins

H.110 Bus Pins	Description
CT_C8_A	8.192 Mhz data clock
CT_C8_B	Redundant 8.192 Mhz data clock
/CT_FRAME_A	8 khz frame clock
/CT_FRAME_B	Redundant 8khz frame clock
CT_NETREF_2	Secondary 8 khz, 1.544 Mhz or 2.048 Mhz telecom network timing reference
CT_MC—2	Mbps message channel
CT_D(N)	8 Mbps data streams
/FR_COMP	8 khz SCBUS compatibility frame clock
SCLK	8.192 Mhz SCBUS compatibility data clock
/CT_EN	Short (level 1) pin to indicate to the CT front board that J4 is fully seated (logical equivalent of the CompactPCI BD_SEL# signal on P1)
/CT_RESET	Reset for use by CT front boards that do not equip J1

Telecom power bus P4 pins

The following pins implement the telecom power supply bus on P4. All telecom power supply pins are level 3, long length.

Note The NP (Not Populated) pins are required to implement the telecom power bus.

Table 14. Description of Telecom power bus

Power Bus	Description
-VBAT	Telecom power source
VBATRTN	Telecom power source return
-SELVBAT	Safety extra low voltage or "short loop" battery (voltage within SELV limits) the –SEL VBAT and SEL VBAT RTN connectors are provided to connect an isolated power source to the backplane for use in powering telephony lines. They are not intended to power the 3U power supplies.
SELVBATRTN	Short loop battery return (voltage within SELV limits)

Support for the telecom power supply consists of 4 separate buses on the backplane, one for each pin as described in Table 14 on page 53.

The –Vbat and VbatRtn telecom power supply buses are qualified to source Unearthed SECONDARY HAZARDOUS voltages as defined by IEC950 and harmonized derivative specifications. The –SELVbat and SELVbatRtn buses are not qualified for SECONDARY HAZARDOUS voltage distribution. Voltage sourced on the –SELVbat bus is within SELV limits.

Telecom ringing bus P4 pins

The following pins are provided for implementing optional ringing voltage buses. All ringing bus pins on P4 are level 2, medium length.

Table 15. Description of telecom ringing bus

Ringing Bus	Description
VRG	Bused ringing voltage source—the VRG and VRGRTN contacts connect a ring voltage source, such as a central office ring signal to the backplane. This is typically 60VRMS—170VRMS, 16Hz to 72Hz.
VRGRTN	Bused ringing voltage return for VRG.

The ringing buses are qualified to source Unearthed SECONDARY HAZARDOUS voltages as defined by IEC950 and harmonized derivative specifications.

Platform power bus P4 pins

The CT bus is connected to all power planes specified below to maintain signal integrity across the P4/J4 connector pair.

Table 16. Power/ground planes on backplane

Power/Ground	Description
+5V	Backplane +5V power plane connection
+3.3V	Backplane +3.3V power plane connection
+12V	Backplane +12V power plane connection
-12V	Backplane –12V power plane connection
V(I/O)	Backplane V(I/O) plane connection
GND	Backplane logic ground plane connection

Shelf enumeration bus P4 pins

The Shelf Enumeration Bus is used for multi-shelf CompactPCI systems. A multi-shelf system comprises multiple sub-racks connected together in a rack or racks. Each sub-rack bus segment can be assigned a shelf address that is bused across each P4 connector position.

The 6U Model 5406 Backplane/Midplane has an S1 header, located at the back of the backplane, on the left-hand side (See figure 17 on page 43). The S1 header has DIP switches labelled SGA0-SGA4, that are user-selectable to set a binary shelf address for each sub-rack. Using various off/on combinations of these SGA switches provides up to 33 (0-32) binary shelf addresses. Table 17 on page 55 lists the 33 switch combinations.

When a switch is placed in the on position, the signal is pulled to ground and is read as a zero by the processor. A switch that is off, would be read as a one. The left position of the S1 header is on, and the right position is off (or “no connect”).

The S1 header selected to shelf address 29 (11101) is shown in figure 18.

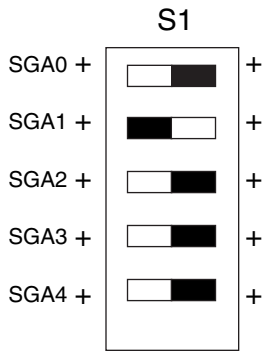


Figure 18. Shelf address switch selected as 29

If geographic addressing (GA0 through GA4) is implemented, the P4 shelf enumeration bus shall also be implemented.

Table 17. Shelf address SGA0–SGA4 switch combinations

16 (SGA4)	8 (SGA3)	4 (SGA2)	2 (SGA1)	1 (SGA0)	Decimal
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	0	0	0	1	17
1	0	0	1	0	18
1	0	0	1	1	19

Table 17. Shelf address SGA0–SGA4 switch combinations (Continued)

16 (SGA4)	8 (SGA3)	4 (SGA2)	2 (SGA1)	1 (SGA0)	Decimal
1	0	1	0	0	20
1	0	1	0	1	21
1	0	1	1	0	22
1	0	1	1	1	23
1	1	0	0	0	24
1	1	0	0	1	25
1	1	0	1	0	26
1	1	0	1	1	27
1	1	1	0	0	28
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31
1	0	0	0	0	32

Geographic address P4 pins

The Geographic slot addresses (GA0 through GA4) are implemented by five level 2, medium length, non-bused pins on each P4 connector. These pins are equivalent to pins specified in the CompactPCI Specification for geographic addressing on P2. The purpose is to provide support for the CompactPCI geographic slot address capability (specified on P2) on CT front boards that may not be equipped with J2.

Note See PICMG, 2.0, R3.0 CompactPCI, Specification for more information

When the shelf enumeration bus (SGA0 through SGA4) is implemented on P4, geographic addressing shall also be available.

Reserved pins on P4

Un-bused, reserved pins (RSVD) are provided on P4 for future CT/telecom applications.

Frame ground bus P4 pins

Frame ground (FG) pins are provided on P4 as a low-impedance return path for transient currents shunted by overvoltage or ESD/EMI protective devices on CT front boards. These pins are connected to the chassis.

FG is considered Earthed SELV and BASIC insulation must exist between it and TNV or SECONDARY HAZARDOUS voltages.

Not populated pins and pads on P4

The 6U Model 5406 Backplane/Midplane meets safety regulatory requirements, as well as eases routing constraints associated with busing the telecom power supply and ringing voltages supply on P4. The entire conductive element of these pins are not populated (NP) where noted (See Table 18 on page 57).

Power fail sense bus pins on P4

The power fail sense bus is implemented on P4 by the following pins: (PFS0# through PFS1#)—Two medium length (level 2) pins, individually bused across each P4 connector position for sensing power supply status.

Table 18. CT H.110 bus P4 pin assignments

PIN	Z	A	B	C	D	E	F
25	NP	SGA4	SGA3	SGA2	SGA1	SGA0	FG
24	NP	GA4	GA3	GA2	GA1	GA0	FG
23	NP	+12V	/CT_RESET	/CT_EN	-12V	CT_MC	FG
22	NP	PFS0#	RSVD	RSVD	RSVD	RSVD	FG
21	NP	-SELVBAT	PFS1#	RSVD	RSVD	SELVBATRTN	FG
20	NP	NP	NP	NP	NP	NP	NP
19	NP	NP	NP	NP	NP	NP	NP
18	NP	VRG	NP	NP	NP	VRGRTN	NP
17	NP	NP	NP	NP	NP	NP	NP
16	NP	NP	NP	NP	NP	NP	NP
15	NP	-VBAT	NP	NP	NP	VBATRTN	NP
12-14	KEY AREA						
11	NP	CT_D29	CT_D30	CT_D31	V(I/O)	/CT_FRAME_A	GND
10	NP	CT_D27	+3.3V	CT_D28	+5V	/CT_FRAME_B	GND
9	NP	CT_D24	CT_D25	CT_D26	GND	/FR_COMP	GND
8	NP	CT_D21	CT_D22	CT_D23	+5V	CT_C8_A	GND
7	NP	CT_D19	+5V	CT_D20	GND	CT_C8_B	GND
6	NP	CT_D16	CT_D17	CT_D18	GND	CT_NETREF_1	GND
5	NP	CT_D13	CT_D14	CT_D15	+3.3V	CT_NETREF_2	GND
4	NP	CT_D11	+5V	CT_D12	+3.3V	SCLK	GND
3	NP	CT_D8	CT_D9	CT_D10	GND	SCLK-D	GND
2	NP	CT_D4	CT_D5	CT_D6	CT_D7	GND	GND
1	NP	CT_D0	+3.3V	CT_D1	CT_D2	CT_D3	GND

Legend

+5V	+5V power	**-Vbat**	Telecom power distribution bus
+3.3V	+3.3V power	**VbatRtn**	Return bus pin for –Vbat
GND	Logic ground	**SGA0-SGA4**	Shelf enumeration bus signals
V(I/O)	I/O cell power	**GA0-GA4**	Slot ID signals; not bused
FG	Frame ground	**VRG**	Bus for ringing voltage
RSVD	Reserved for future use	**VRGRtn**	Return bus pin for VRG
NP	A pin and pad to "Not be Populated"	**PFS0#-PFS1#**	Buses for power fail sense
-SELVbat	Short loop battery	**Key Area**	Area utilized for coding key
SELVbatRtn	Short loop battery return		

Key electrical considerations

Timing considerations limit the CT bus length to a maximum of 21 plug-in board slots. Board-to-board spacing is 0.8 inch, with a maximum allowance of 4-inch traces between slots 7 and 8, and between slots 14 and 15. Connectors are of the 2mm HM 5-row family. Table 7 provides a list of key electrical considerations for the CT bus.

Table 19. Key electrical considerations for the CT bus

Item	Parameters
Signal line impedance	65Ω
Maximum number of slots	21
Plug-in board pitch	0.8 inches
Maximum trace length between segments	4 inches
Connectors	5-row, 2mm HM
Clock termination	100Ω/100 Pf AC
Plug-in board series terminations (clock)	33Ω (in parallel with a series switch)
Series switch state	Open, except on the controller board
Plug-in board pull-down resistor (clock line)	10 kΩ to 0.0V
Plug-in board pull-up resistor (data line)	18 kΩ to 0.7V
Maximum plug-in board stub (clock)	2 inches
Maximum plug-in board stub (data)	4 inches
Plug-in board series termination (data)	24Ω

User-defined CT I/O on P5

If the CT bus is implemented on J4/P4, telephony I/O can be implemented on J5/P5. Since there is a wide-range of non-CT boards that may use the J5/P5 connectors, there is no specific backplane customization for telecom I/O. Patton's 6U Model 5406 Backplane/Midplane is in compliance with the *CompactPCI Computer Telephony Specification*, which guarantees that no signals will be bused across P5 on CT slots in the backplane.

The P5 pins are user-defined for through-backplane analog and digital telephony I/O, user-definable I/O, and CT front board supply voltage feed-through. Additionally, P5 connectors have staged front side pins to provide hot-swap capability.

To meet certain safety regulatory agency requirements relative to telephony line (tip and ring pairs), certain pins in P5 are required to have no connection made to them. The Insulation-No-Connect (IN/C) pins are required to meet insulation spacing requirements relative to TNV.

Pin assignments are specified in the *Computer Telephony Specification* for P5 that will support up to 24 TNV3-2-1-SELV telephony connections or up to 32 TNV1-SELV telephony connections. Since there are various types of line interfaces on CT front boards and the different safety requirements placed on these interfaces, many different mappings of tip/ring signals to the J5/P5 connector is possible.

It should be noted, however, that the specification allows for exclusive use of J5/P5 for a single TNV classification. That is, for a given CT Front Board and/or backplane slot, P5 should be used exclusively for TNV3, OR for TNV2, OR for TNV1, OR for SELV classified telephony signals. Care must be taken when mixing differ-

ent levels of TNV classification within the tip-ring block of pins on P5 due to the insulation spacing requirements and voltage breakdown requirements of many safety regulatory agencies.

Note Refer to the *PICMG, 2.5 R1.0 CompactPCI, Computer Telephony Specification* for more information

In order to guarantee that non-CT I/O boards, using J5 for general purpose I/O and designed to meet only minimal safety requirements, are not plugged in to backplane slots that could be rear wired for TNV 3-2-1 voltage levels, System Integrators should use front panel keying (See “Front panel and cardguide keys” on page 49.)

Chapter 6 Maintenance

Chapter contents

Troubleshooting

System won't power up

If the green LED on the power supply module does not light up, you should:

Turn off the power supply module's front panel switch, and remove it from the chassis (warm-swap). Then plug it back in, making sure it is seated properly. Flip the switch to "on". If green LED still does not light up, check to make sure the polarity is wired correctly at the back of the chassis.

If the green LED lights up on the power supply module, but the system still isn't powering-up, then the module may be faulty and should be returned to the manufacturer.

Hot-swap of power supply fails

The power supply module is designed for a warm-swap, and should not be hot-swapped. To warm-swap the power supply module, simply turn the power switch to "off" on the front panel prior to removal/insertion. If it has been hot-swapped and is not working, turn the switch "off" and remove it from the chassis. Allow a minute or two for the module to cool down, then plug it back in with the switch "off". Once it is seated, turn switch on.

No-load condition generates a false alarm

The power supply module may generate a false alarm under a no-load condition (no cards installed). A minimum of 1/2 amp (system admin card would suffice) needs to be plugged into the sub-rack to prevent this false alarm.

Warranty Information

Patton Electronics Co. warrants all components to be free from defects, and will—at our option—repair or replace the product should it fail within one year from the first date of shipment.

This warranty is limited to defects in workmanship or materials, and does not cover customer damage, abuse or unauthorized modification. If this product fails or does not perform as warranted, your sole recourse shall be repair or replacement as described above. Under no condition shall Patton Electronics Co. be liable for any damages incurred by the use of this product. These damages include, but are not limited to, the following: lost profits, lost savings and incidental or consequential damages arising from the use of or inability to use this product.

Patton Electronics Co. specifically disclaims all other warranties, expressed or implied, and the installation or use of this product shall be deemed an acceptance of these terms by the user.

Service

All warranty and non-warranty repairs must be returned freight prepaid and insured to Patton Electronics. All returns must have a Return Materials Authorization number on the outside of the shipping container. This number may be obtained from Patton Electronics Technical Support at:

tel: **(301) 975-1007**
E-mail: **support@patton.com**
www: **http://www.patton.com**

Note Packages received without an RMA number will not be accepted.

Patton Electronics' technical staff is also available to answer any questions that might arise concerning the installation or use of your product. Technical Services hours: **8AM to 5PM EST, Monday through Friday**.

Appendix A **Glossary of Terms**

Chapter contents

C

CFM
Cubic feet per minute—A measurement of how much air is moved through a fan.

CSA
Canadian Standards Association—Organization which operates a listing service for electrical and electronic materials and equipment. It is the body that establishes telephone equipment (and other) standards for use in Canada.

CT
Computer Telephony—is the adding of computer intelligence to the making, receiving, and managing of telephone calls.

D

Dual Redundant
An environment containing two power supplies, with fault tolerance such that one power supply may fail and the system will continue to operate.

E

ECTF
Enterprise Computer Telephony Forum—A nonprofit corporation formed to focus on the technical challenges of interoperability among Computer Telephony Integration (CTI) products.

EIA
Electronics Industry Association—Trade organization of manufacturers which sets standards for use of its member companies.

EMC
Electromagnetic Compatibility—Is the ability of equipment or systems to be used in their intended environment within designed efficiency levels without causing or receiving degradation due to unintentional EMI.

EMI
Electromagnetic Interference—any electromagnetic interference, periodic or random, narrow or broadband, which may have a disturbing influence on devices exposed to it.

EN
European Norms—Prefix assigned to documents adopted by the CE designating required standards (for example, EN 60950 is the safety specification (equivalent to UL 1950)).

Enumeration
The action taken by the Host to poll the configuration spaces of the PCI devices and allocate (deallocate) the necessary resources (memory and/or I/O address space, interrupts, software drivers).

ESD
Electrostatic Discharge—Discharge of a static charge on a surface or body through a conductive path to ground. Can be damaging to integrated circuits.

Eurocard
A series of mechanical board form factor sizes for rack-based systems.

H

Hot-Swap
The capability of removing and replacing components without turning off the system. Hot-swap capability is increasingly important in systems used for applications such as telecommunications, which require that the system be operational at some level continuously.

HP
Horizontal Positioning—A unit of measurement used for the width of CPCI cards/modules. 1 HP = 0.2” wide

I

IDE
Integrated Drive Electronics—a hard disk drive standard interface for PCs.

IEC
International Electrotechnical Committee

IEEE
Institute of Electrical and Electronics Engineers

IN/C
Insulation No Connect—required for safety agency insulation requirements.

ISA
Industry Standard Architecture—A specification by which Personal Computers (PCs) add boards.

K

Keying
A mechanical means of polarizing connectors in order to prevent similar connectors from being mated. This is necessary when 2 or more similar connectors must be connected to a backplane which requires that the board being connected is unique for a particular slot.

N

N+1 Redundant
An environment containing more than two power supplies, where the power supplies typically current share, with fault tolerance such that one power supply may fail and the system will continue to operate.

NEBS
Network Equipment Building Standards—Defines a rigid and extensive set of performance, quality, environmental and safety requirements developed by Bellcore, the R&D and standards organization owned by the seven regional Bell operating companies (RBOC's).

NP
Not Populated—pins within connector that must not be populated due to safety requirements.

P

PCI
Peripheral Component Interconnect. A specification for defining between logic components. Typically used for interconnecting high-speed, PC-compatible chipset components. The PCI specification is issued through the PCI Special Interest Group (PCI SIG).

PCI SIG
Peripheral Component Interconnect Special Interest Group

PICMG
PCI Industrial Computers Manufacturers Group—a consortium of industrial computer product vendors who develop specifications for PCI-based systems and boards for use in industrial computing applications.

Platform
Describes the system environment, including the backplane and related enclosure.

S

SELV
Safety Extra Low Voltage—a term generally defined by the regulatory agencies as the highest voltage that can be contacted by a person and not cause injury. It is often specifically defined as 30 VAC or 42.4 VDC.

S-HAZ
Secondary Hazardous—any voltage within a system that is greater than 60VDC (42.4VAC-peak), NOT meeting the requirements for a LIMITED CURRENT CIRCUIT, or for a TNV CIRCUIT. Typical ringing voltage is considered SECONDARY HAZARDOUS unless it is current limited. Raw ringing is considered SECONDARY HAZARDOUS. (Refer to IEC950 or PICMG 2.5 R1.0 CompactPCI, Computer Telephony Specification for information.)

Shroud
A male connector body designed to fit over the extended tails of a long tail connector which allows a female connector to be mated from the rear side for midplane or rear I/O applications.

T

TDM
Time Division Multiplex—A technique for transmitting a number of separate data, voice and/or video signals simultaneously over one communications medium by quickly interleaving a piece of each signal one after another.

TNV
Telephone Network Voltages—any voltage present on the telephone network side of the isolation device on any device (for example, board) that connects to the telephone network.

U

U
An EIA unit of measurement equal to 1.75” for equipment racks.

W

Warm-Swap
An environment supporting removal and insertion of power supplies while under power, wherein the power supply is disabled during insertion and removal, avoiding the need for the connectors to make and break high current connections while under load.